Internal electromagnetic immunity model for analog circuits

Advisors: Geneviève Duchamp, Alain Meresse, Jean-Luc Levant

Industrial partner: ATMEL Nantes

Phd context (1)

- Integrated Circuit as microcontrollers
  - Proximity between analog and digital parts
  - Working frequency rising
  - Supply voltage falling
  - Decrease of margin voltage

- Risk of EM interference

- Analog function failure
  - Critical for security equipment
**Integrated Circuits Electromagnetic Compatibility (EMC) improvement**
- To limit disturbance emission
- To avoid of functional failures

**EMC standards for Integrated Circuits**
- Emissivity: \textit{ICEM-CE} [1]
- Immunity: \textit{ICIM-CI} [2] (New proposal)

- \textit{Estimate analog circuit immunity with ICIM-CI methodology}
- \textit{Improve function reliability and specification}

---

**Analog to digital Converter immunity model**
- ICIM-CI methodology
- Model created from the design
- ADC study
- Functional failure study

- Study of the disturbance propagation inside the circuit
- Sensitive circuit pointed out
Whole ADC ICIM-CI model

- PDN model
  - Packaging Model
  - Coupling path model
- Immunity Behavioral Model
  - Functional model
  - Immunity control block
- Immunity parameter extraction
- Immunity voltage curves for criteria

Main results

- Whole conversion process immunity analysis
- Determination of the disturbance voltage needed to lose $2^N$ LSB ($N \in [0,10]$)
- Input voltage customizable
- Different immunity behaviors pointed out
Publications


Perspective

Whole ADC ICIM-CI Model designed
Good results compared with the measurements
Package model
  • Allowing chip external disturbing

➢ Integration of ICIM methodology in the ATMEL design flow for ADC designs
➢ Improve the analog design, improve the PCB filter

➢ Next step: Immunity model of another analog devices