The DPI Immunity Behavior of Microcontrollers

Tao Su
Markus Unger
Thomas Steinecke
Infineon Technologies AG, Germany

Robert Weigel
University of Erlangen-Nuremberg, Germany
Contents

- Introduction
  - State of the art, problems, motivation and research plan
- Properties of the immunity of microcontrollers
  - Base immunity and immunity drops
- Foot-point immunity drop
  - Assumption
  - Verification
  - Improvement
  - Simulation
- PDN immunity drop
- Conclusion
Introduction: State of the Art and problems

- Immunity of complex ICs like microcontrollers
  - Test Method
    - Issue: Repeatable and comparable measurement
    - Progress: Standard: RF immunity (IEC62132), Pulse immunity (draft)
    - Problem: Variations in the test setup, test software and failure criteria
  - Modelling
    - Issue: Model simplification and system level model
    - Progress: On-chip and on-board power distribution network
    - Problem:
      - No idea of the correct model structure
      - Poor correlation between the simulation and the measurement
  - Design
    - Problem: No guideline, No platform
Introduction: Motivation and Research Plan

- **Motivation:**
  - The determining factors for the immunity

- **Disturbance Injection Method**
  - Direct power injection (DPI, IEC 62132-4)
  - 0.5 MHz ~ 1 GHz

- **Systematic analysis**
  - Pin type
  - Pin location
  - Pin load
  - System frequency
  - Different microcontrollers
Properties of Immunity

- Test on digital I/O pins
  - Base immunity
    - 1 ~ 10 MHz range
    - High coupling coefficient
    - Determined by supply voltage, driver current, digital transition threshold
  - High frequency drops
    - Above 100 MHz range
    - Even lower than the base immunity
Properties of Immunity: Immunity Drop

Immunity drops are common for all pin types and all microcontrollers

**C161 (0.45 µm)**
- VDD: 5 V

**XC2287 (0.13 µm)**
- VDDPA: 5 V
- VDDPB: 5 V
- VDDI1: 1.5 V
- VDDIM: 1.5 V

**XC161 (0.25 µm)**
- VDDI: 2.5 V

**TC1767 (0.13 µm)**
- VDDP: 3.3 V
- VDD: 1.5 V
- VDDOSC33: 3.3 V
- VDDOSC: 1.5 V

**TC1767 (D I/O: 3.3 V)**

**XC2287 (D I/O: 5 V)**
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Properties of Immunity: Immunity Drop

- Possible origins of the immunity drop
  - Semiconductor material
    - Energy band → $f >> 1$ GHz
  - Metal-semiconductor structures
    - Deep submicron meter cavity → $f >> 1$ GHz
  - Passive network
    - Disturbance injection network: no influence
    - **Power distribution network**: (more at the end)
    - **Signal distribution network**: maybe but where?
Foot-Point Immunity Drop: Property

- Correlation between immunity drops and the load of the oscillator pin
  - → Foot-point immunity drop!
  - How to calculate the frequency?

<table>
<thead>
<tr>
<th>No.</th>
<th>Colour of the curve</th>
<th>Foot-point capacitor at XTAL1</th>
<th>Foot-point capacitor at XTAL2</th>
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<tbody>
<tr>
<td>1</td>
<td>Red</td>
<td>6.8 pF</td>
<td>6.8 pF</td>
</tr>
<tr>
<td>2</td>
<td>Blue</td>
<td>6.8 pF + 10 pF</td>
<td>6.8 pF</td>
</tr>
<tr>
<td>3</td>
<td>Green</td>
<td>6.8 pF</td>
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Foot-point Immunity Drop: Origin

- Foot-point diagram of the oscillator pin

Impedance $Z_{\text{chip}}$ vs. Frequency

S11 vs. Frequency

Immunity $\sim f_{pkx1}$ vs. Frequency

Diagram showing the impedance $Z_{\text{chip}}$ and $Z_{\text{board}}$ as functions of frequency, along with S11 and immunity graphs. The diagram also illustrates the components within a microcontroller and the ground of printed circuit board with very low impedance.
Verification of the foot-point diagram

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Foot-Point Immunity Drop: Origin

- Foot-point diagram of the supply and the digital I/O pins
  - Common current loop
    - Same foot-point frequency

![Diagram showing foot-point diagram of the supply and digital I/O pins, highlighting oscillator I/O, common current loop, and same foot-point frequency.](image)
Foot-Point Immunity Drop: Improvement

- PCB design
  - Reduce the loop inductance
  - However, limited by chip itself
    - chip limit \( f_{cl} = \frac{1.07\text{GHz}}{\sqrt{\frac{L_{pkg.v1} C_{pad.vss.x1}}{5nH} \frac{1}{2pF}}} \)

PCB Layout

```
Crystal
Foot-point capacitor
Additional grounding
```

![Graphs showing forward power vs. frequency for 400 MHz, 800 MHz, and 900 MHz](image)
Foot-point Immunity Drop: Simulation

Supply pin

Oscillator input pin

Digital I/O pin

Oscillator output pin

Red: measurement
Blue: simulation
PDN Immunity Drop: Property

- High frequency immunity drop correlated to S11 on the supply pin

**Graph:**
- Frequency (MHz) on the x-axis
- Forward Power (dBm) on the y-axis
- S11 on the y-axis

**Legend:**
- Red: add all DeCap 300 nF
- Green: add remote DeCap 200 nF
- Blue: add local DeCap 100 nF
- Black: no DeCap

**Diagram:**
- VDD, VSS, VDD supply layers
- Ground layer
- Disturbance points
- DeCap locations

**Notes:**
- The DPI Immunity Behavior of Microcontrollers
Simple conductive current loops can explain the PDN immunity drop up to 100 MHz, but cannot predict the frequency of the drop above the 100 MHz range.
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Loop resonance below 100 MHz
Simple conductive current loops can explain the PDN immunity drop up to 100 MHz, but cannot predict the frequency of the drop above the 100 MHz range.

Possible reason: efficient field coupling between the chip and the PCB

- New method to model the chip-PCB coupling
- New philosophy of modelling

\[ f = \frac{1}{2\pi \sqrt{2nH \times 50pF}} \approx 500MHz \]
Conclusion

- The immunity of microcontrollers can be characterized with the base immunity and the immunity drops.

- Immunity drops are divided into the foot-point immunity drop and the PDN immunity drop. Both drops come from resonances in current loops in the passive network of the microcontroller system.

- The immunity drop is related to the impedance structure of the microcontroller system including the chip and the board. That property challenges the reproducibility and comparability of the immunity test method above 100 MHz.

- Immunity modelling should include the foot-point diagram and the PDN diagram. The current modelling philosophy, that the chip model and the board model are created separately, is questionable.