

3 The MOS modeling

This chapter introduces the CMOS transistor modeling. The static characteristics of n-channel and p-channel MOS devices are shown, with details on the maximum current and its relationship with the sizing, the threshold voltage and various 2nd order effects. Three generations of MOS device models are introduced. Firstly, the original MOS model 1 is presented, as it was proposed in the early versions of SPICE simulator developed by the University of Berkeley, California. We demonstrate the inaccuracies of this model. Secondly, we introduce the semi-empirical model 3, which is still in use for MOS device simulation with a channel length greater than 1 μ m. Thirdly, we present a simplified version of the BSIM4 models, developed by the University of Berkeley for MOS devices with channel length down to 90nm.

Details on model parameters are provided for all models. The effects of temperature on the MOS performances are then presented. Finally, the three different MOS that may be found in 0.12 μ m are introduced: low threshold voltage, high speed and high voltage.

1. Introduction to modeling

Modeling the MOS device consists in writing a set of equations that link voltages and currents, in order to simulate and predict the behavior of the single device [Shockley] and consequently the behavior of a complete circuit. A considerable research and development effort has been dedicated in the past years to modeling MOS devices in an accurate way. Many books have been published over the years about the semiconductor physics and semiconductor device modeling. The most common references are [Tsividis], [Sze], [Lee] and recently [Liu]. For MOS devices, one of the key objectives of the model is to evaluate the current I_{ds} which flows between the drain and the source, depending on the supply voltages V_d, V_g, V_s and V_b .

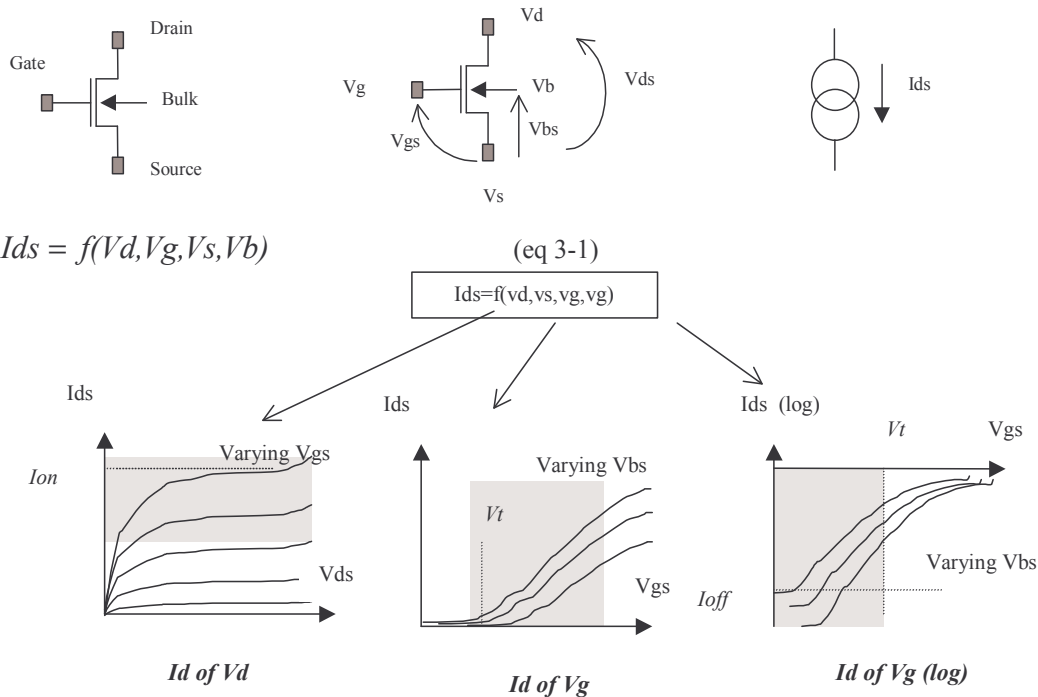


Figure 3-1: Useful representations of the MOS device characteristics

From the equation (3-1), we may represent the variation of the current I_{ds} versus voltages in three different ways, as illustrated in figure 3-1. The graphs are usually called I_d/V_d , I_d/V_g , and $I_d(\log)/V_g$. For simplicity's sake, we consider that the voltage V_s is grounded.

In the I_d/V_d curve, the current I_{ds} is plotted for varying gate voltage V_{gs} , from 0 to VDD. The parameter I_{on} gives the maximum available current, corresponding to maximum voltage V_{ds} and V_{gs} . I_{on} is a very important parameter for signal switching, for example in logic gates.

In the I_d/V_g curve, we extract the threshold voltage. In the previous chapter we observed the parasitic effects due to this threshold. Analog design is much concerned by an accurate prediction of the threshold voltage.

Then, the curve $I_d(\log)/V_g$ is convenient to illustrate the current I_{ds} for small values of the gate control. One of the most important parameters is the I_{off} current, when $V_g=0$, that has a direct impact on standby power consumption.

A second objective of MOS models is to estimate the value of parasitic capacitances, mainly C_{gs} , C_{gd} and C_{gb} (Figure 3-2). Those capacitance prove to vary with the voltage V_s, V_d, V_g and V_b . Although not considered in the static simulations I_d/V_d and I_d/V_g , the variation of the capacitance must be computed at each iteration of the analog simulation, for accurate prediction of the switching delay.

$$C_{gs} = f_1(V_d, V_g, V_s, V_b) \quad (\text{eq 3-2})$$

$$C_{gd} = f_2(V_d, V_g, V_s, V_b) \quad (\text{eq 3-3})$$

$$C_{gb} = f_3(V_d, V_g, V_s, V_b) \quad (\text{eq 3-4})$$

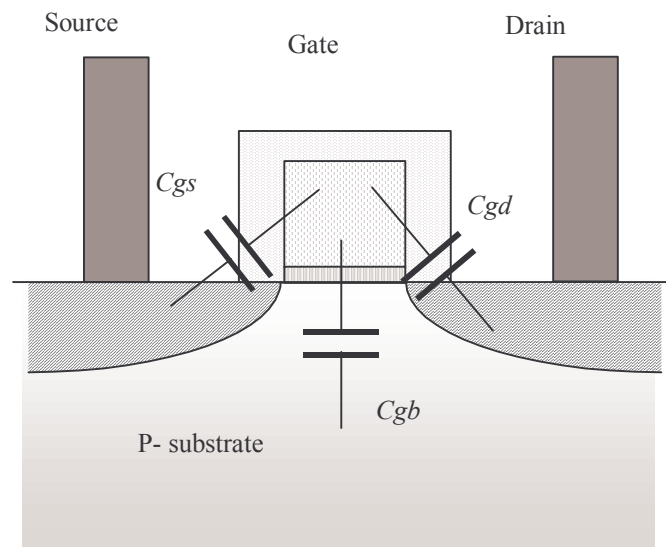


Figure 3-2: Capacitance between the gate and the source, drain, or substrate

A long list of MOS models have been developed for analog simulators. We choose to implement in Microwind2 three of those: the model 1, the model 3 and the model BSIM4. Details on those three models and their physical basis are provided in the next paragraphs.

The complete set of parameters for a given technology is called the model card. The procedure to build an accurate MOS model is quite complex, as it is based on a large set of measurements and sophisticated optimization procedures. The experimental data concerning a MOS device with large width and large length is used first, to fix basic parameters. Then the MOS model is tuned for small channel device measurements, and then for several sizes.

2. MOS Model 1

Equations

Historically, the MOS model 1 was the first to be proposed by Shockley, in 1952 [Shockley]. The equations of the MOS level 1 are provided in the next paragraphs. The evaluation of the current I_{ds} between the drain and the source as a function of V_d, V_g and V_s is summarized in equations 3-5, 3-6 and 3-7. The model parameters appearing in the user interface of Microwind2 are written using COURRIER font. The device operation is divided into three regions: cut-off, linear and saturated.

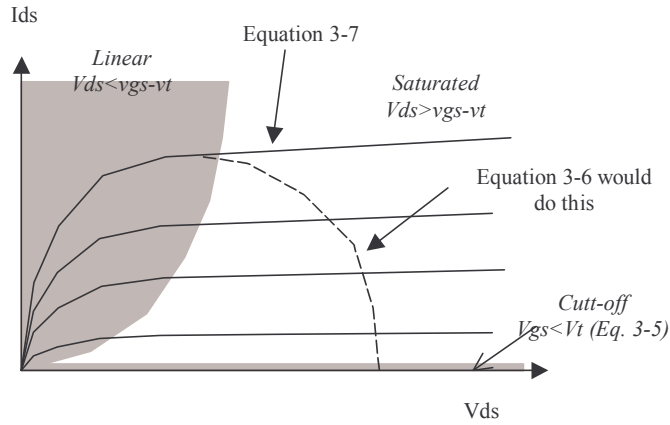


Figure 3-3: Two main domains are considered in the model: the linear area and the saturated area.

IF $V_{gs} < 0$, the device is in cut-off mode.

$$I_{ds} = 0 \tag{3-5}$$

IF $V_{ds} < V_{gs} - V_{TO}$, the device is in linear mode

$$I_{ds} = U_0 \frac{\epsilon_0 \epsilon_r}{TOX} \cdot \frac{W}{L} \left((V_{gs} - vt) \cdot V_{ds} - \frac{(V_{ds})^2}{2} \right) \tag{3-6}$$

IF $V_{ds} > V_{gs} - V_{TO}$, the device is in saturated mode:

$$I_{ds} = U_0 \frac{\epsilon_0 \epsilon_r}{TOX} \cdot \frac{W}{L} (V_{gs} - vt)^2 \tag{3-7}$$

With:

$$vt = V_{TO} + GAMMA(\sqrt{(PHI - vbs)} - \sqrt{PHI}) \tag{3-8}$$

$\epsilon_0 = 8.85 \cdot 10^{-12}$ F/m is the absolute permittivity

ϵ_r = relative permittivity, equal to 3.9 in the case of SiO2 (no unit)

Mos Model 1 parameters			
Parameter	Definition	Typical Value 0.12µm	
		NMOS	PMOS
VTO	Theshold voltage	0.4V	-0.4V
U0	Carrier mobility	0.06m ² /V-s	0.02m ² /V-s
TOX	Gate oxide thickness	2nm	2nm
PHI	Surface potential at strong inversion	0.3V	0.3V
GAMMA	Bulk threshold parameter	0.4 V ^{0.5}	0.4 V ^{0.5}
W	MOS channel width	1µm	1µm
L	MOS channel length	0.12µm	0.12µm

Table 3-1: Parameters of MOS level 1 implemented into Microwind2

Implementation in Microwind

The static characteristics of the MOS model 1 may be obtained using the command **Simulate → Mos characteristics** available in the main menu of Microwind.

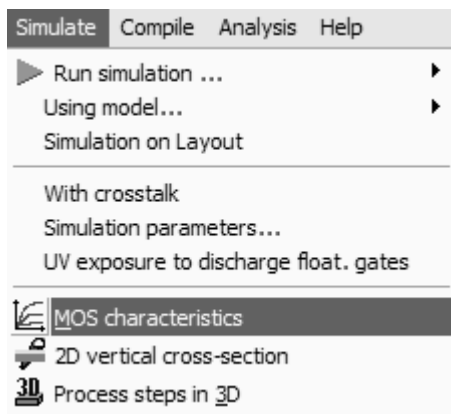


Figure 3-4: Access to the static MOS characteristics

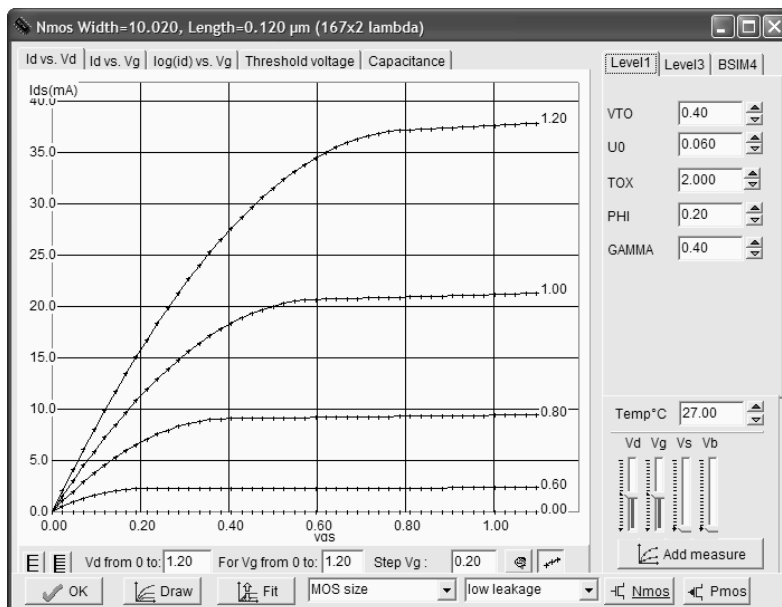


Figure 3-5: The screen used to simulate the static characteristics of the MOS with model 1 within Microwind2

In the top right part of the window, select the item "Level 1". The variation of I_{ds} versus the voltage V_{ds} , for varying gate voltage V_{gs} , is shown by default. The device width is $10\mu\text{m}$ by default, the channel length is $0.12\mu\text{m}$. The parameters VTO, U0, TOX, PHI and GAMMA are listed in the right part of the window.

Mismatch between simulation and measurements

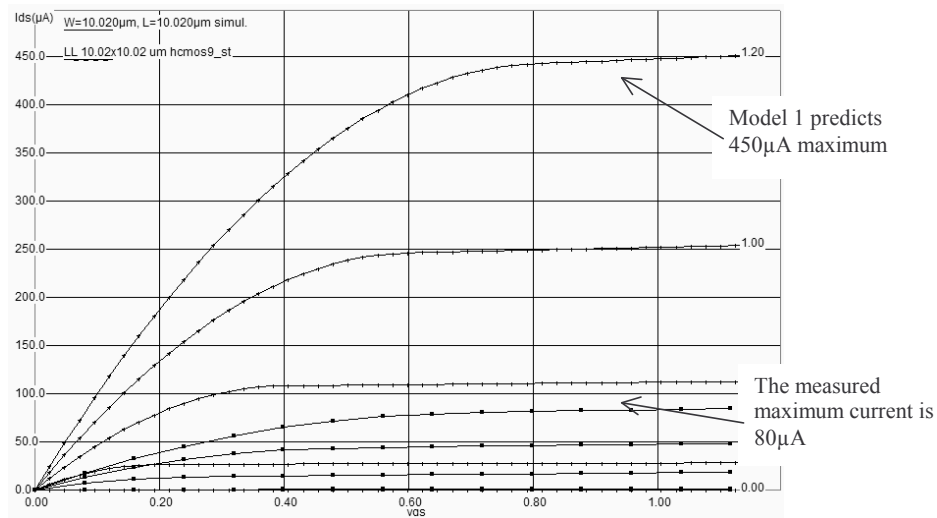


Figure 3-6: The model 1 predict a current 5 times higher than the measurement in the case of a large channel MOS device ($L=10\mu\text{m}$).

These old equations (1968, in [Shichman]) are not acceptable in $0.12\mu\text{m}$. If we consider MOS devices with very long lengths ($L>10\mu\text{m}$), the mismatch between the simulation and the measurement is of the order of a factor of five. Let us compare the simulation and the measurement, for a device with a width $W=10\mu\text{m}$, and a long channel length $L=10\mu\text{m}$, fabricated in $0.12\mu\text{m}$ CMOS technology, as presented in figure 3-6. The measurement *Ne10x10.MES* was downloaded using the button **Load Measurement**. This measurement corresponds to an n-channel MOS device with a $10\mu\text{m}$ channel width and $10\mu\text{m}$ length, fabricated in CMOS $0.12\mu\text{m}$ from ST-microelectronics.

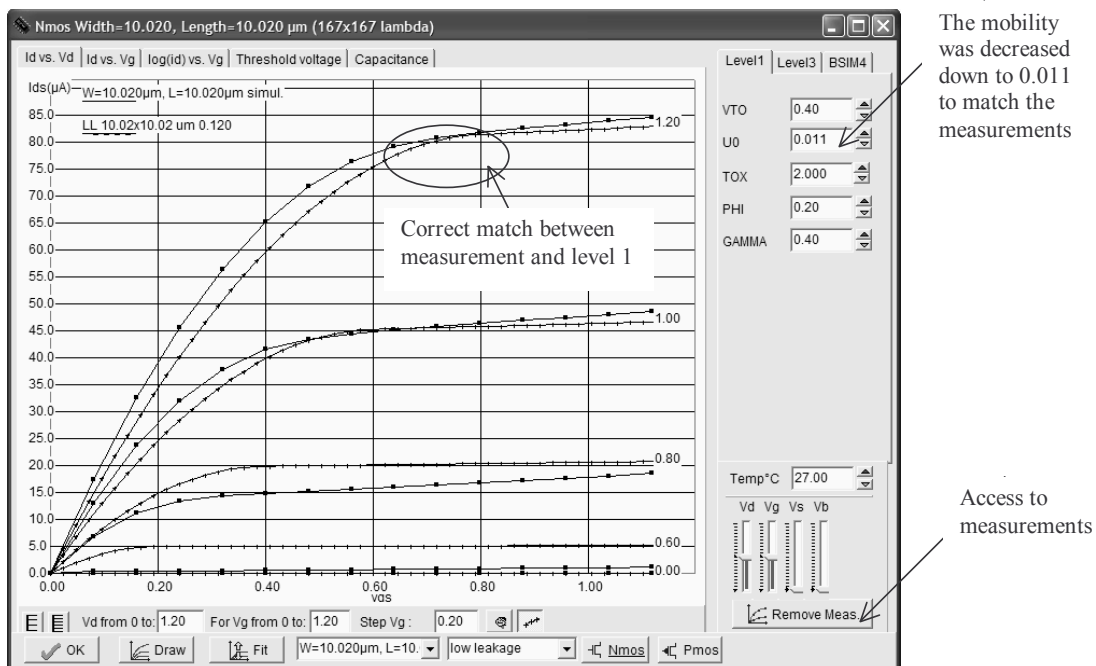


Figure 3-7: Comparing measured I_d/V_d and level 1 simulations for a $10 \times 10 \mu\text{m}$ device result in a surprising similarity (Ne10x10.MES).

Initially, the simulation and measurement do not correspond at all. The mobility U_0 needs to be decreased from its initial value 0.06 down to 0.01. The curves are fitted at the price of an unrealistic change in the mobility parameter.

When dealing with sub-micron technology, the current predicted by model "Level 1" is several times higher than the real-case measurements. This means that several parasitic effects appeared with the technology scale down, most of them tending to reduce the effective current compared to the early modeling equations of model 1.

3. MOS Model 3

For the evaluation of the current I_{ds} as a function of V_d, V_g and V_s between drain and source, we commonly use the following equations, close to SPICE model 3 formulations. The formulations are derived from model 1 and take into account a set of physical limitations in a semi-empirical way.

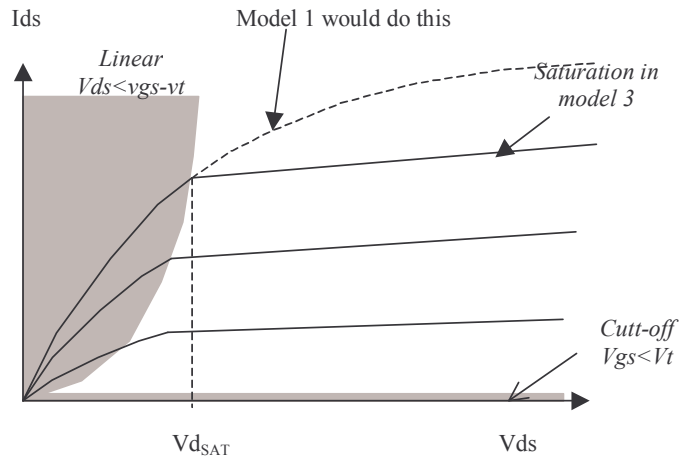


Figure 3-8: Introduction of the saturation voltage Vd_{SAT} which truncates the equations issued from model 1

One of the most important change is the introduction of Vd_{SAT} , a saturation voltage from which the current saturates and do not rise as the LEVEL1 model would do. This saturation effect is significant for small channel length. The main LEVEL3 equations are listed below.

CUT-OFF MODE. $V_{gs} < 0$

$$I_{ds} = 0 \tag{3-9}$$

NORMAL MODE. $V_{gs} > V_{on}$

$$I_{ds} = K_{eff} \frac{W}{L_{eff}} (1 + KAPPA \cdot V_{ds}) V_{de} \left((V_{gs} - V_{th}) - \frac{V_{de}}{2} \right) \tag{3-10}$$

with

$$V_{on} = 1.2V_{th}$$

$$V_{th} = V_{TO} + GAMMA(\sqrt{PHI - V_{bs}} - \sqrt{PHI})$$

$$V_{de} = \min(V_{ds}, V_{dsat})$$

$$V_{dsat} = V_c + V_{sat} - \sqrt{V_c^2 + V_{sat}^2}$$

$$V_{dsat} = V_{gs} - V_{th}$$

$$V_c = V_{MAX} \frac{L_{eff}}{0.06}$$

$$L_{eff} = L - 2LD$$

The formulation of the effective factor K_{eff} (Equation 3-11) includes a mobility degradation factor θ , which tends to reduce the mobility at high V_{gs} . The consequence is a reduction of the current I_{ds} as compared to $LEVEL1$.

$$K_{eff} = \frac{\epsilon_0 \epsilon_r \mu_0}{t_{OX} (1 + \theta (v_{gs} - v_{th}))} \quad (3-11)$$

In sub-threshold mode, that is for a gate voltage less than the threshold voltage, V_{ds} is replaced by V_{on} in the above equations. An exponential dependence of the current with V_{gs} is introduced by using the equation 3-12. Notice the temperature effect introduced in the denominator nkT .

Without any voltage applied to the gate, the current is no more equal to zero. The current of I_{ds} for $V_{gs}=0$ is called the I_{off} current (Figure 3-9). Its value in $0.12\mu m$ is around 10^{-10} A. In contrast, for $V_{gs}=V_{DD}$, the maximum current I_{on} is of the order of several mA (10^{-3} A).

$$I_{ds} = I_{ds}(V_{on}, V_{ds}) \exp\left(\frac{q(V_{gs} - V_{on})}{nkT}\right) \quad (3-12)$$

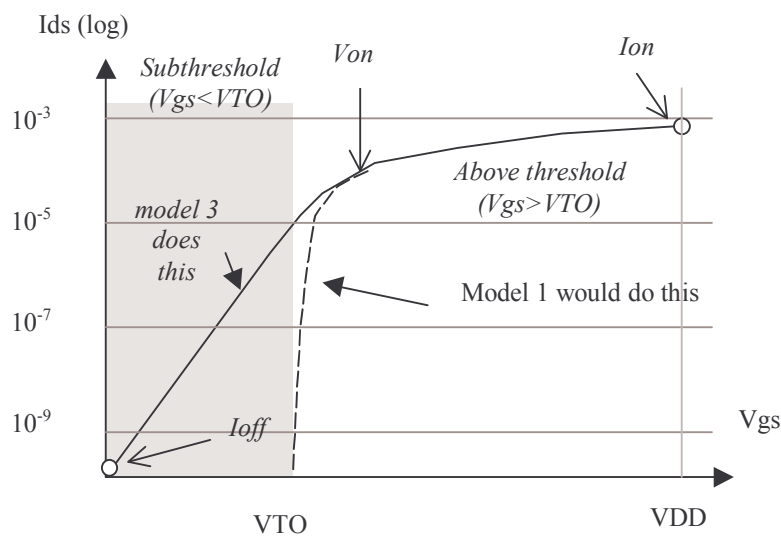


Figure 3-9: Introduction of an exponential law to model the sub-threshold behavior of the current

TEMPERATURE EFFECTS

The MOS device is sensitive to temperature. Three main parameters are concerned: the threshold voltage V_{TO} , the mobility μ_0 and the slope in sub-threshold mode dependent on kT/q . Both V_{TO} and μ_0 decrease when the temperature increases. The physical background is the degradation of the mobility of electrons

and holes when the temperature increase, due to a higher atomic volume of the crystal underneath the gate, and consequently less space for the current carriers. The modeling of the temperature effect is as follows:

$$U0 = U0_{(T=27)} \left(\frac{T + 273}{300} \right)^{-1.5} \tag{eq. 3-13}$$

$$VT = VT0_{(T=27)} - 0.002(T - 300) \tag{eq. 3-14}$$

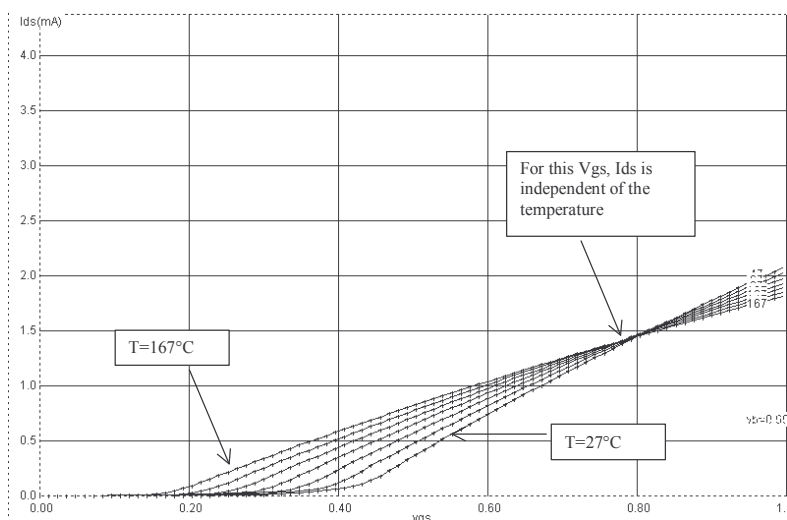
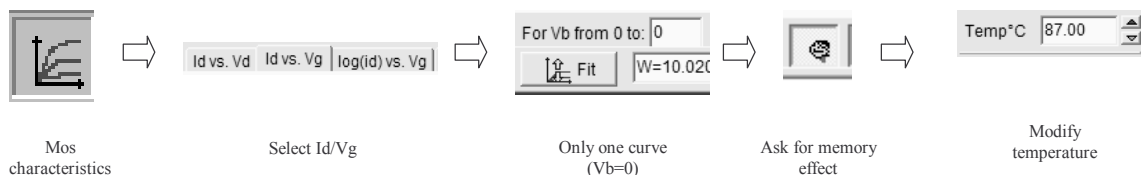


Figure 3-10 The effect of temperature on the MOS characteristics. In Id/Vg mode, a specific Vds makes the current independent of the temperature.

To obtain the curve of figure 3-10, click the icon MOS characteristics, select the curve Id/Vg, and enter the value "0" for the upper limit of Vb, so as to draw only one single curve. Enable the screen memory mode by a click on the icon **Enable Memory**. When you change the temperature, the change in the slope and the temperature-independent point appear, as shown in figure 3-10.

Mos Model 3 parameters			
Parameter	Definition	Typical Value 0.12µm	
		NMOS	pMOS
VTO	Theshold voltage of a long channel device, at zero Vbs.	0.4V	-0.4V
U0	Carrier mobility	0.06 m ² /V.s	0.025 m ² /V.s
TOX	Gate oxide thickness	3 nm	3 nm
PHI	Surface potential at strong inversion	0.3V	0.3V

LD	Lateral diffusion into channel	0.01 μm	0.01 μm
GAMMA	Bulk threshold parameter	0.4 $\text{V}^{0.5}$	0.4 $\text{V}^{0.5}$
KAPPA	Saturation field factor	0.01 V^{-1}	0.01 V^{-1}
VMAX	Maximum drift velocity	150Km/s	100Km/s
THETA	Mobility degradation factor	0.3 V^{-1}	0.3 V^{-1}
NSS	Subthreshold factor	0.07 V^{-1}	0.07 V^{-1}
W	MOS channel width	0.5-20 μm	0.5-40 μm
L	MOS channel length	0.12 μm	0.12 μm

Table 3-xxx: list of parameters used in the implementation of the LEVEL3 model in Microwind2

Microwind User's Interface

You may understand the action of each parameter by using the screen reported in figure 3-11. Each parameter may be changed interactively using cursors, or by entering with the keyboard the appropriate value.

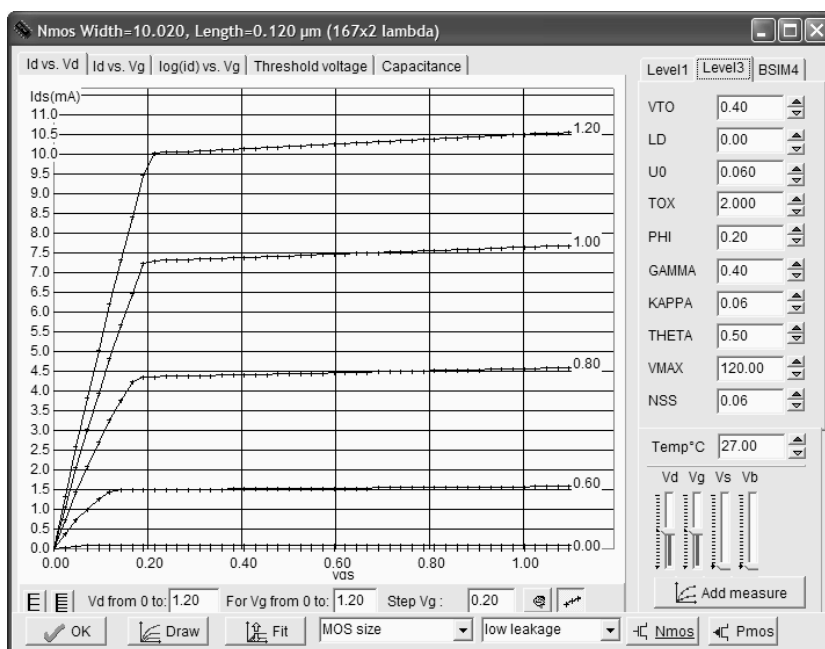


Fig. 3-11. The user interface to investigate the effect of each parameter on the current I_{ds} ($W=10\mu\text{m}$, $L=0.12\mu\text{m}$)

Several screens may be proposed:

- I_d vs. V_d , for varying V_g . This is the default screen. Its main interest is the characterization of the Ion current, the maximum current available in the device, for V_d and V_g set to VDD.
- I_d vs. V_g , for varying V_b . In this screen, the threshold voltage V_t (VTO) is characterized, as well as its dependence on the bulk polarization.
- I_d vs. V_g , in logarithmic scale. This screen is mandatory to characterize the MOS device in sub-threshold mode, that is for $V_{gs} < V_t$. Two of the important parameters are the slope of the current vs.

V_{gs} , and the I_{off} current. The I_{off} current is the standby current appearing between drain and source for $V_{gs}=0$.

- Threshold voltage V_t vs. $Length$. This screen has been added to illustrate advances in the modeling of deep-submicron effects. With LEVEL 3, V_t is constant for varying length, but is impacted by the bulk voltage.
- $Capacitance$ vs. V_{ds} . This screen illustrates the variation of C_{gs} and C_{gd} versus the drain-source voltage.

Current versus drain-source voltage

Using the display mode **Id vs. Vd**, you may see the effect of parameters U_0 , TOX , $KAPPA$ and $VMAX$. Basically, the carrier mobility U_0 moves the whole curve, as it impacts the current I_{ds} in an almost linear way. As U_0 is nearly a physical constant, a significant change of mobility has no physical meaning. The oxide thickness TOX does the same but in an opposite way.

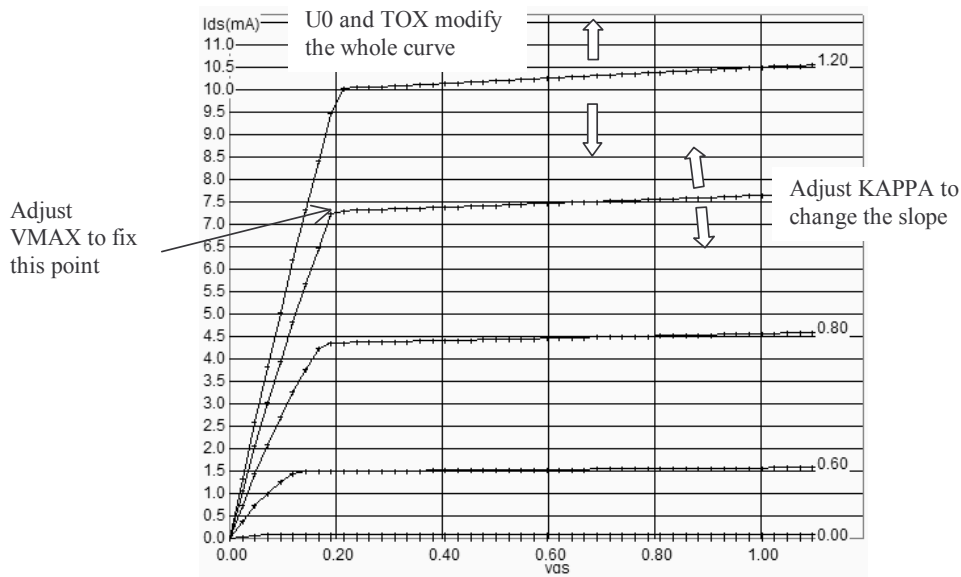


Fig. 3-12. Demonstration of the role of U_0 , $KAPPA$ and $VMAX$ in I_d/V_d ($W=10\mu m$, $L=0.12\mu m$)

A TOX increase leads to a less efficient device, with less current. $KAPPA$ changes the slope of the current when V_{ds} is high, corresponding to the saturation region. Finally, $VMAX$ truncates the curves for low values of V_{ds} , to fit the transition point between the linear and the saturated region (Figure 3-12).

Current versus gate voltage

The role of V_{TO} and $GAMMA$ can be observed in the figure 3-13, using the display mode I_d vs. V_g . If we use a long channel device, that is a length much greater than the minimum length, the second order effects are minimized. Act on V_{TO} cursors in order to shift the curves right or left, and $GAMMA$ to fit the spacing between curves. Parameters U_0 and T_{OX} also have a direct impact on the slope for high V_{gs} .

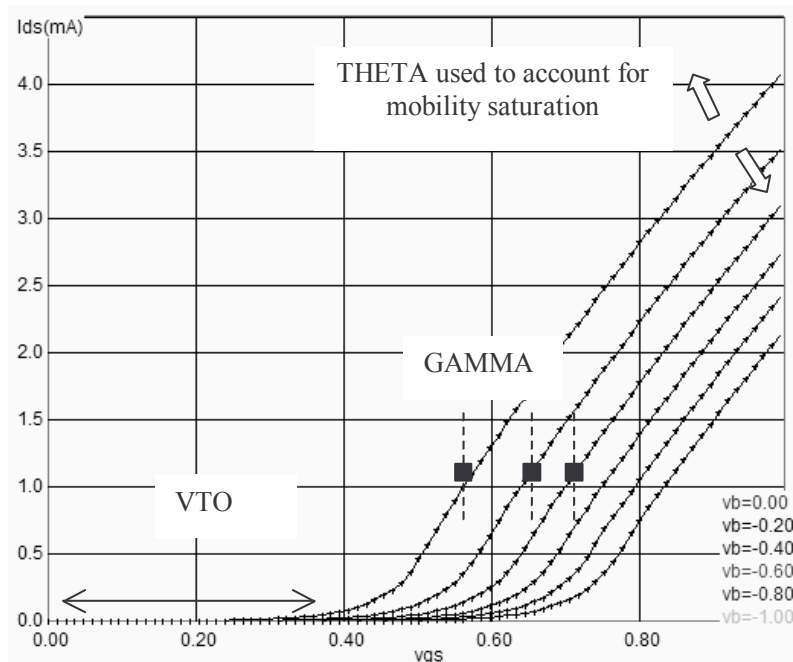


Fig. 3-13. The effects of V_{TO} and $GAMMA$ are illustrated in I_d/V_g mode voltage ($W=10\mu m$, $L=0.12\mu m$)

Now we focus on a short channel MOS device, for example $W=2\mu m$, $L=0.12\mu m$. Using the same display mode I_d vs. V_g , we obtain similar curves as for long-channel device. We observe that the shape of the current is bent. This modification is due to short channel parasitic effects. The parameter $THETA$ is used to bend the current curves at high V_{gs} . The MOS model 3 do not provide parameters to account for the V_{TO} dependence with length.

Current vs V_g in logarithmic scale

We finally illustrate the role of NSS in the display mode $I_d(\log)/V_g$ (Figure 3-14). The parameter NSS has a direct impact on the slope in sub-threshold mode, that is for $V_{gs} < V_t$.

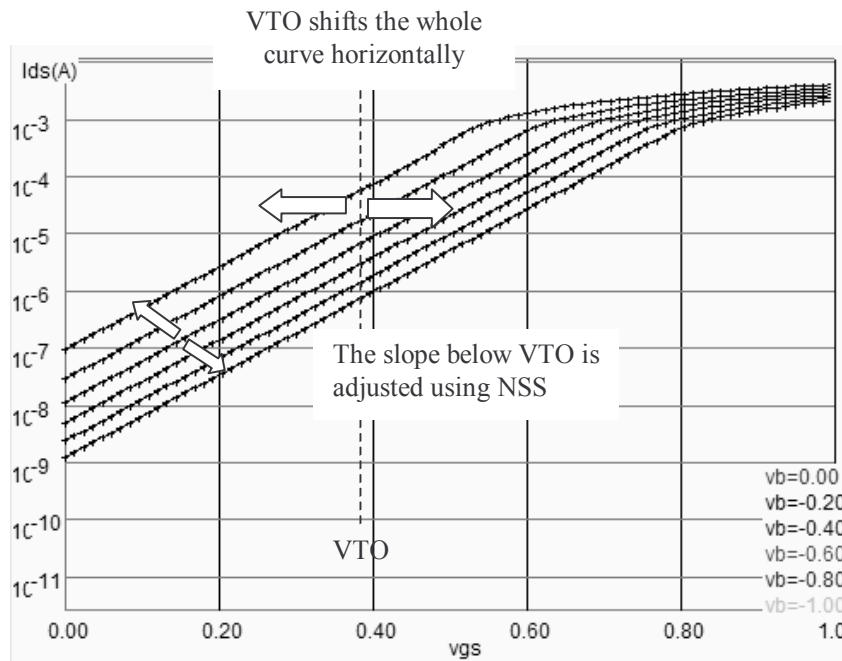


Figure 3-14. In sub-threshold region, the I_d dependence on V_{gs} is exponential. The slope is tuned by parameter NSS . The whole curve is shifted using V_{TO} voltage ($W=10\mu m$, $L=0.12\mu m$)

Capacitance vs. V_{ds}

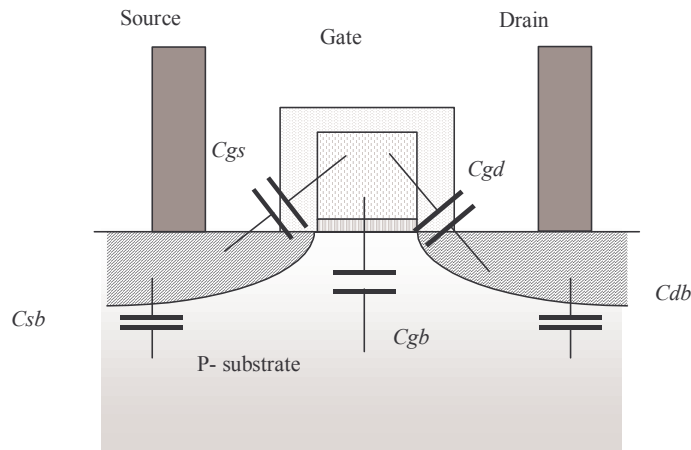


Figure 3-15: The MOS capacitance considered in MOS model 3

The five main capacitors considered in our implementation of MOS model 3 are the gate to bulk capacitance C_{gb} , the gate to source capacitance C_{gs} , the gate-to-drain capacitance C_{gd} , the junction capacitance between source and bulk C_{sb} and the junction capacitance between drain and bulk C_{db} .

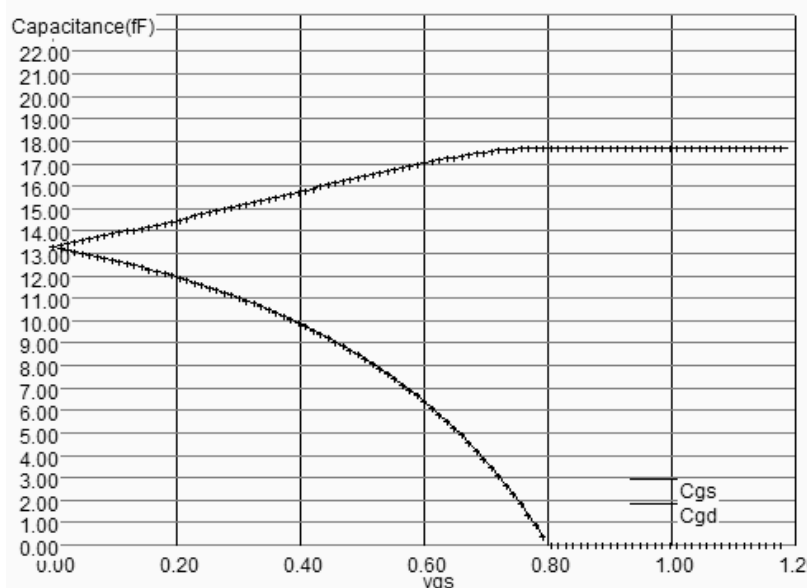


Figure 3-16: The evolution of MOS capacitance with the drain voltage ($W=10\mu\text{m}$, $L=0.12\mu\text{m}$)

The variation of the capacitance must be computed at each iteration of the analog simulation, for accurate prediction of the switching delay. In our implementation of MOS level 3, we use the following model, based on the formulations given in [Fjedly]. The parameter V_{dsat} was given by equation 3-10.

$$C_{GS} = \frac{2}{3} C_i \left[1 - \left(\frac{V_{GS} - V_t - V_{dsat}}{2(V_{GS} - V_t) - V_{dsat}} \right)^2 \right] \quad (3-15)$$

$$C_{GD} = \frac{2}{3} C_i \left[1 - \left(\frac{V_{GS} - V_t}{2(V_{GS} - V_t) - V_{dsat}} \right)^2 \right] \quad (3-16)$$

$$C_{GB} = 0 \quad (3-17)$$

with

$$C_i = W.L. \frac{\epsilon_0 \epsilon_r}{\text{TOX}} \quad (3-18)$$

W = width of the MOS device (m)

L = length of the MOS device (m)

TOX = oxide thickness (m)

The two remaining capacitance C_{DB} and C_{SB} are junction capacitance. Their model is given by equations 3-19 and 3-20.

$$C_{DB} = W.L_{drain} \frac{CJ}{\left(1 - \frac{V_{BD}}{PB} \right)^{MJ}} \quad (3-19)$$

$$C_{SB} = W \cdot L_{source} \frac{CJ}{\left(1 - \frac{V_{BS}}{PB}\right)^{MJ}} \tag{3-20}$$

where

W is the channel width (m)

L_{drain} is the drain length, according to figure 3-17 (m)

CJ is around 3×10^{-4} F/m²

PB is the built-in potential of the junction (around 0.8V)

MJ is the grading coefficient of the junction (around 0.5)

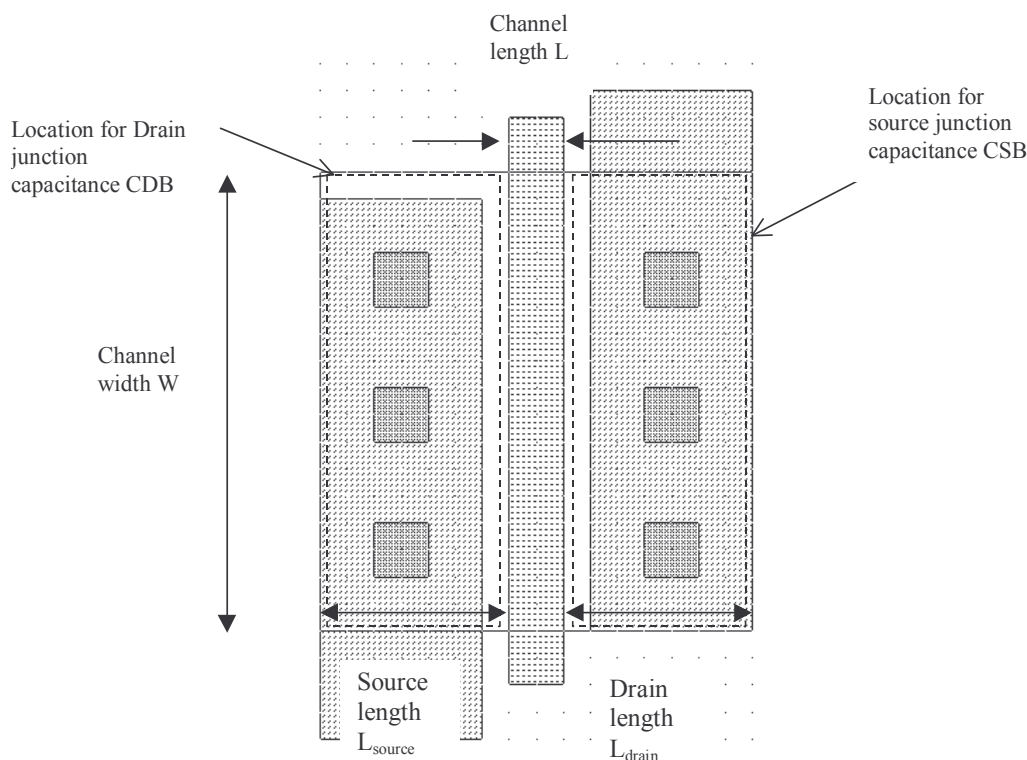


Figure 3-17: The junction capacitance for drain and source contributes significantly to the MOS capacitance

4. The BSIM4 MOS Model

A family of models has been developed at the University of Berkeley for the accurate simulation of sub-micron and deep submicron technologies. The Berkeley Short-channel IGFET Model (BSIM) exists in several versions (BSIM1, BSIM2, BSIM3). The BSIM3v3 version, promoted by the Electronic Industries Alliance (EIA) is an industry standard for deep-submicron device simulation [Eia].

A new MOS model, called BSIM4 [Bsim4], was introduced in 2000. A simplified version of this model is supported by Microwind2, and recommended for ultra-deep submicron technology simulation. The complete details on BSIM4 are provided in the excellent book [Liu]. BSIM4 still considers the operating regions described in MOS level 3 (linear for low V_{ds} , saturated for high V_{ds} , subthreshold for $V_{gs} < V_t$), but provides a perfect continuity between these regions. BSIM4 introduces a new region where the impact ionization effect is dominant (Figure 3-18). In that region, V_{ds} is very high, over the nominal supply voltage VDD. One of the key features of BSIM4 is the use of one single equation to build the current, valid for all operating modes. Smoothing functions ensure a nice continuity between operating domains.

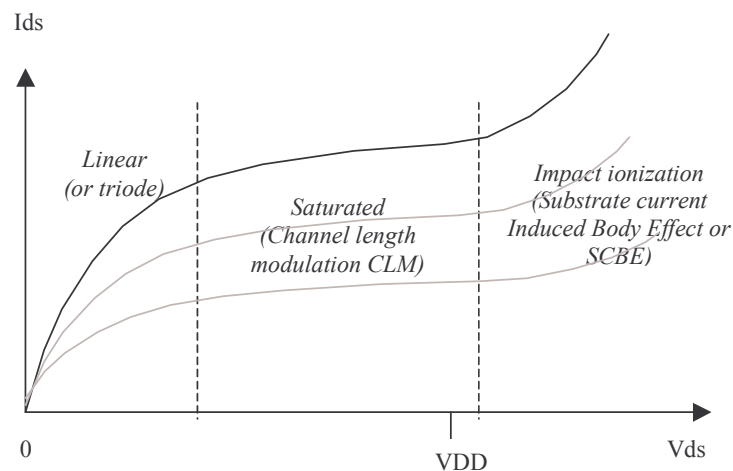


Figure 3-18: The three regions considered in our simplified version of BSIM4

The number of parameters specified in the official release of BSIM4 is as high as 300. A significant portion of these parameters is unused in our implementation. We concentrate on the most significant parameters, for educational purposes. The set of parameters is reduced to around 30.

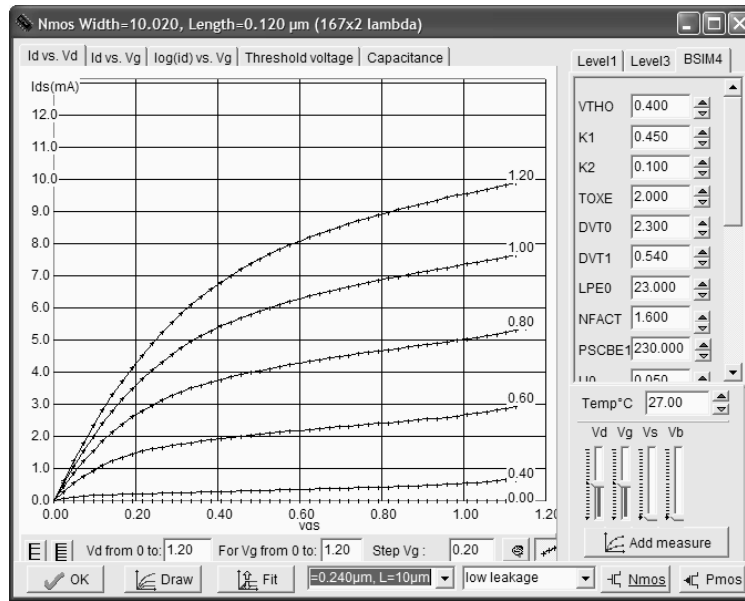


Figure 3-19: Implementation of BSIM4 within Microwind2, based on [Liu]

Effective Channel Length and Width

Once fabricated, the physical length L_{eff} and width W_{eff} of the MOS device do not correspond exactly to the initial length L and width W drawn using Microwind2 (Figure 3-20). The parameters L_{INT} and W_{INT} have been introduced for that purpose, with equations 3-21 and 3-22.

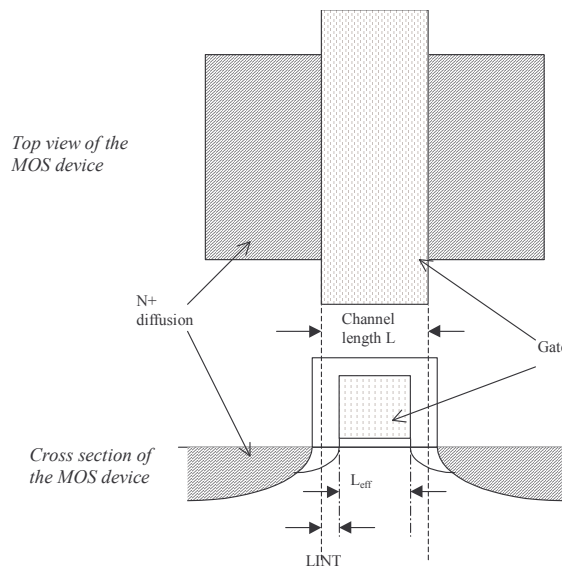


Figure 3-20: Illustration of the effective channel length L_{eff}

$$L_{eff} = L - 2.LINT \quad (3-21)$$

$$W_{eff} = W - 2.WINT \quad (3-22)$$

Surface potential and junction depth

The surface potential Φ_s and junction depth are basic parameters taken into account in the evaluation of the threshold voltage and the global current. The surface potential Φ_s is defined by equation 3-23.

$$\Phi_s = 0.4 + vt \cdot \ln\left(\frac{NDEP}{ni}\right) \quad (3-23)$$

where vt the thermal voltage given by equation 3-24, $NDEP$ is the channel doping concentration for zero body bias (Around 10^{17}cm^{-3} in practice), and ni is the intrinsic carrier concentration of silicon ($ni=1.02 \times 10^{10}\text{cm}^{-3}$ at 300°K). Consequently, the surface potential Φ_s in deep-submicron CMOS process is around 0.85V.

The thermal voltage is

$$vt = \frac{k_B T}{q} \quad (3-24)$$

k_B = Boltzmann constant = 1.38×10^{-23} J/K

T = temperature (300°K by default)

q = Electronic charge = 1.60×10^{-19} C

The built-in voltage of the source/drain junctions is given by equation 3-25.

$$V_{bi} = vt \cdot \ln\left(\frac{NDEP \cdot NSD}{ni^2}\right) \quad (3-25)$$

where vt the thermal voltage given by equation 3-24, $NDEP$ is the channel doping concentration for zero body bias (Around 10^{17}cm^{-3} in practice), NSD is the source/drain doping concentration (Around 10^{20}cm^{-3} in practice), and ni is the intrinsic carrier concentration of silicon ($ni=1.02 \times 10^{10}\text{cm}^{-3}$ at 300°K). Consequently, the built-in voltage V_{bi} in deep-submicron CMOS process is around 1.0V.

The depletion depth X_{dep} is computed by equation 3-26. It corresponds to the thickness of the region near the N+/P- junction interfaces, as illustrated in figure 3-21.

$$X_{dep} = \sqrt{\frac{2\varepsilon_{rsi} \cdot \varepsilon_0 (\Phi_s - V_{bs})}{q \cdot NDEP}} \quad (3-26)$$

where ϵ_{rsi} is the dielectric constant of silicon (11.7) ϵ_0 is the permittivity in vacuum ($8.854 \times 10^{-12} \text{F/m}$), Φ_s is the surface potential given by equation 3-23, N_{DEP} is the channel doping concentration for zero body bias, q is the electronic charge ($1.60 \times 10^{-19} \text{C}$), and v_{bs} is the bulk-source potential. The typical value of X_{dep} is $0.5 \mu\text{m}$ (Figure 3-21).

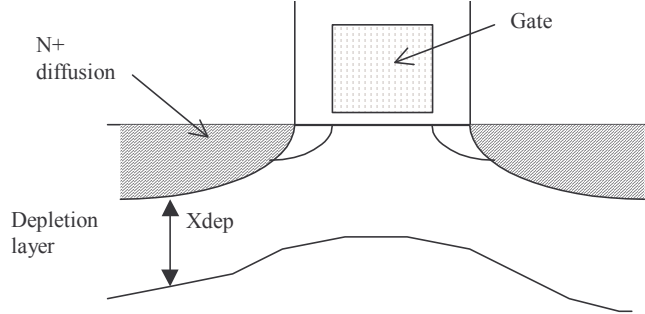


Figure 3-21: Illustration of the depletion depth X_{dep}

Threshold voltage

The main impact of the threshold voltage V_t is the I_{off} parasitic current, that exhibits an exponential dependence with $1/V_t$. A high threshold voltage V_t leads to a small I_{off} current, at the price of a low I_{on} current. Low threshold MOS devices consume a very high standby current, which impacts the power consumption of the whole circuit. An accurate prediction of the threshold voltage is a key issue for low power integrated circuit design. The general equation of the threshold voltage is presented in equation 3-27.

$$v_{th} = V_{TH0} + K_1 \sqrt{(\Phi_s - V_{bs}) - \sqrt{\Phi_s}} - K_2 V_{bs} + \Delta V_{t_{SCE}} + \Delta V_{t_{NULD}} + \Delta V_{t_{DIBL}} \quad (3-27)$$

where V_{TH0} is the long channel threshold voltage at $V_{bs}=0$ (Around 0.5V), K_1 is the first order body bias coefficient ($0.5 \text{ V}^{1/2}$), Φ_s is the surface potential given by equation 3-23, V_{bs} is the bulk-source voltage, K_2 is the second order body bias coefficient, $\Delta V_{t_{SCE}}$ is the short channel effect (SCE <gloss>) on V_t (Detailed in equation 3-28), $\Delta V_{t_{NULD}}$ is the non-uniform lateral doping effect (NULD <gloss>) explained in equation 3-29, and $\Delta V_{t_{DIBL}}$ is the drain-induced barrier lowering (DIBL <gloss>) effect of short channel on V_t (Detailed in equation 3-30).

Short channel effect

The threshold voltage is not the same for all MOS devices. There is a complex dependence between the threshold voltage and the effective length of the channel. For small channel, the threshold value tends to decrease. The equation 3-28 is proposed, based on an hyperbolic cosine function.

$$\Delta V_{t_{SCE}} = - \frac{0.5 \cdot DVT_0}{\cosh(DVT_1 \cdot \frac{L_{eff}}{l_t} - 1)} (V_{bi} - \Phi_s) \quad (3-28)$$

where $DVT0$ is the first coefficient of short-channel effect on the threshold voltage (2.2 by default), $DVT1$ is the second coefficient of short-channel effect on the threshold voltage (0.53 by default), L_{eff} is the effective channel length given in equation 3-21, and l_t is the characteristic length, approximated in our implementation to 1/4 of the minimum channel length ($0.03 \mu\text{m}$ for a $0.12\mu\text{m}$), V_{bi} is defined in equation 3-25, and Φ_s is the surface potential given by equation 3-23.

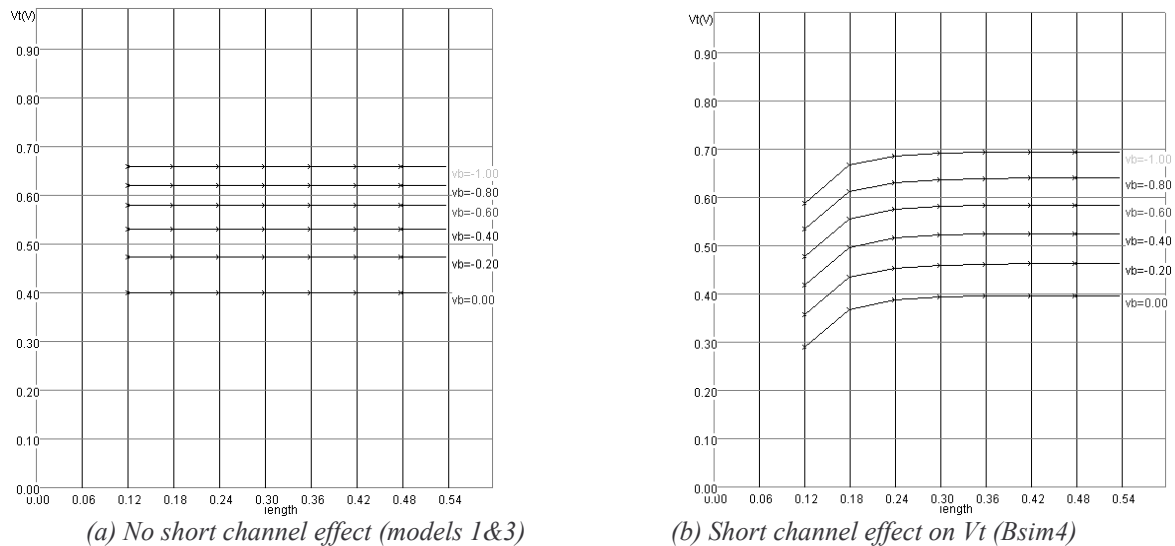


Fig. 3-22: Short channel effect (SCE) on the threshold voltage

The illustration of the effect of $\Delta V_{t_{SCE}}$ is proposed in figure 3-22. Without taking into account the short-channel effect, the threshold voltage is only dependent on V_{bs} . It can be seen that V_t increases when V_{bs} decreases. There is no dependence on the length. When we add the contribution of the short-channel effect expressed by equation 3-28, the threshold voltage is decreased significantly for small length values.

Non-uniform lateral doping

The lateral drain diffusion (LDD) is a technique introduced in recent technologies to reduce the peak channel fields in the MOS channel. The location for high-field parasitic effects is illustrated in the process section of figure 3-23 (a).

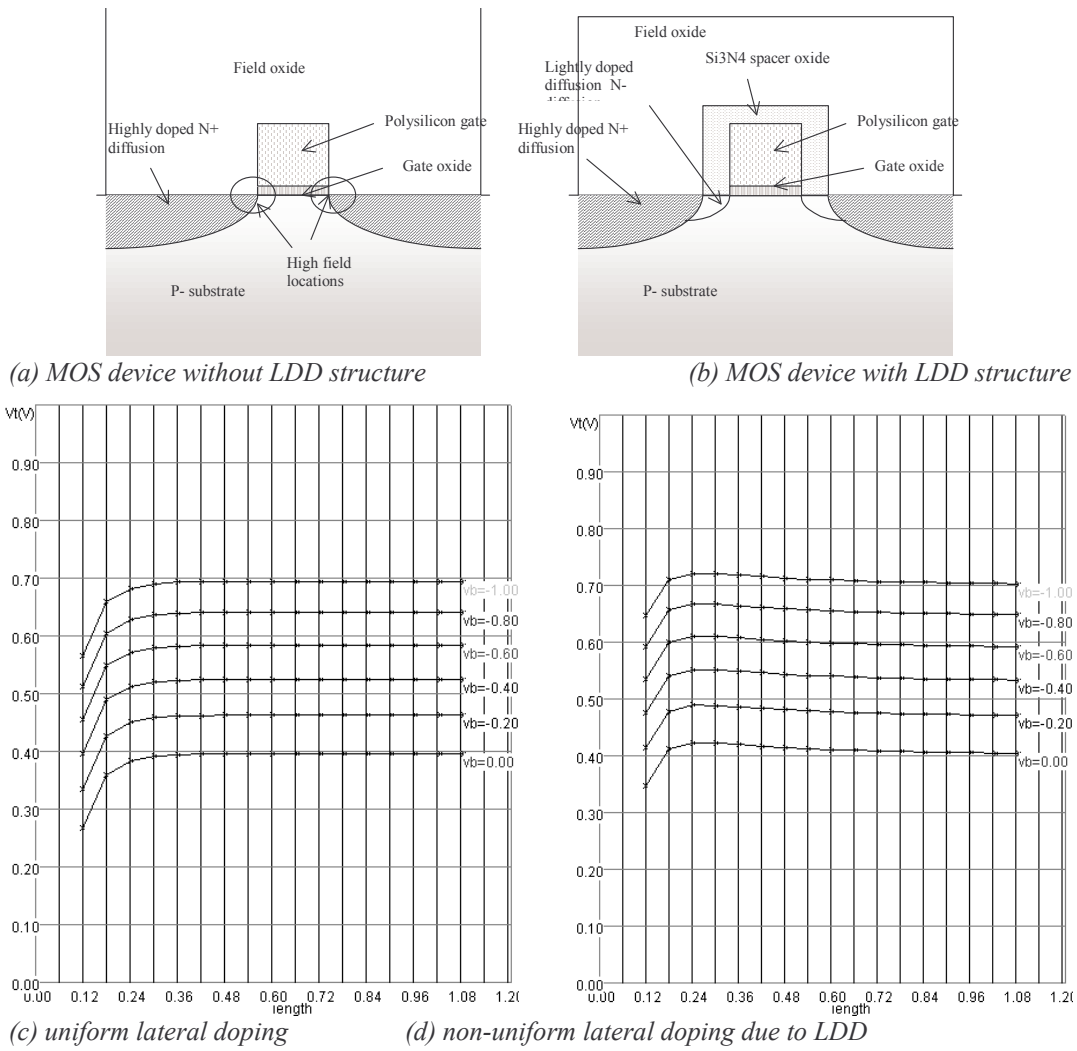


Fig. 3-23: Effect of non-uniform lateral doping on the threshold dependence with the channel length

In the cross-section of figure 3-23 (b), the doping concentration at the corner of the gate is reduced thanks to a lightly doped N-type implantation. The Si3N4 spacer is grown over the gate before the N+ highly doped implantation is performed. Consequently, the high-field effects are moderated. Unfortunately, the threshold voltage exhibits a complex dependence on the channel length, as illustrated in figure 3-23 (d), compared to (c). For a decreasing length, the threshold voltage tends to increase first (due to $\Delta V_{t_{NULD}}$), before decreasing rapidly due to the short channel effect $\Delta V_{t_{SCE}}$ described in formula 3-28.

A simple formulation of the non-uniform lateral doping is $\Delta V_{t_{NULD}}$ given below:

$$\Delta V_{t_{NULD}} = K1 \left(\sqrt{1 + \frac{LPE0}{L_{eff}}} - 1 \right) \cdot \sqrt{\Phi_s} \quad (3-29)$$

Drain induced barrier lowering

When we apply a positive voltage on the drain of a long-channel n-MOS device, we observe no significant change in the value of V_t . When we do the same for a short-channel n-MOS device, we observe a decrease of the threshold voltage. The physical origin of DIBL is the increase of the depletion layer due to a high value of V_{ds} that reduces the equivalent channel length, and consequently decreases the threshold voltage [Liu].

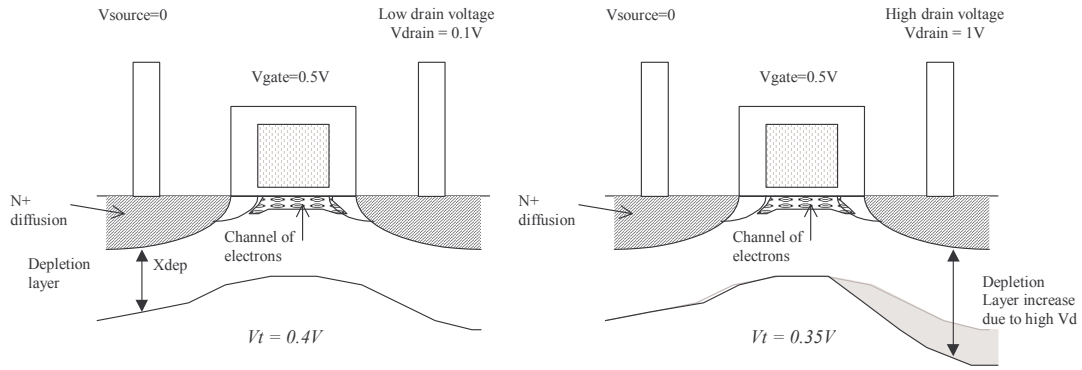


Fig. 3-24: Illustration of the depletion depth X_{dep}

$$\Delta V_{t_{DIBL}} = -0.5 \cdot ETA0 \cdot V_{ds} \tag{3-30}$$

A simplified model of the DIBL effect on the threshold voltage is proposed in equation 3-30. The parameter $ETA0$ is the DIBL coefficient in sub-threshold region (default value 0.08), and V_{ds} is the drain-source voltage.

Mobility

In this paragraph, we introduce the formulations for mobility of channel carriers. The generic parameter is $U0$, the mobility of electrons and holes. The effective mobility μ_{eff} is reduced due to several effects: the bulk polarization, and the gate voltage. The equation implemented in Microwind2 is one of the mobility models proposed in BSIM4 (Equation 3-31).

$$\mu_{eff} = \frac{U0}{1 + (UA + UC \cdot V_{BS}) \left(\frac{V_{gsteff} + 2(V_{TH0} - V_{fb} - \phi_s)}{TOXE} \right)^{EU}} \tag{3-31}$$

where

$U0$ is the low field mobility, in $m^2/V\cdot s$. Its default value is around 0.06 for n-channel MOS and 0.025 for p-channel MOS.

UA is the first order mobility degradation coefficient, in m/V . Its default value is around 10^{-15} .

UC is the body-effect coefficient of mobility degradation, in m/V^2 . Its default value is -0.045×10^{-15} .

V_{FB} is the flat band voltage, in V. It is computed using equation 3-32, where Φ_S is derived from equation 3-23. Its value is around 0.8V.

$$V_{FB} = V_{TO} - \Phi_S - K1\sqrt{\Phi_S} \quad (3-32)$$

$TOXE$ is the oxide thickness, in m. A typical value for $TOXE$ in 0.12 μ m is 2nm ($2 \cdot 10^{-9}$ m).

V_{BS} is the voltage difference between the bulk and the source (V).

EU is a coefficient equal to 1.67 for n-channel MOS, and 1.0 for p-channel MOS.

The parameter $V_{gst_{eff}}$ is a smoothing function, to ensure continuity between the subthreshold region and the linear region.

$$V_{gst_{eff}} = \max(V_{OFF}, \frac{n \cdot vt \cdot \ln(1 + \exp(\frac{V_{gs} - V_{th}}{n \cdot vt}))}{1 + n \cdot \exp(\frac{-(V_{gs} - V_{th})}{n \cdot vt})}) \quad (3-33)$$

$$n = 1 + NFACTOR \quad (3-34)$$

A specific parameter V_{OFF} is introduced to account for a specific effect appearing in short-channel device when V_{gs} is negative. Conventional models predict that the current decrease with an exponential law down to zero with decreasing V_{gs} . For $V_{gs} < 0$, I_{ds} is supposed to be 0.

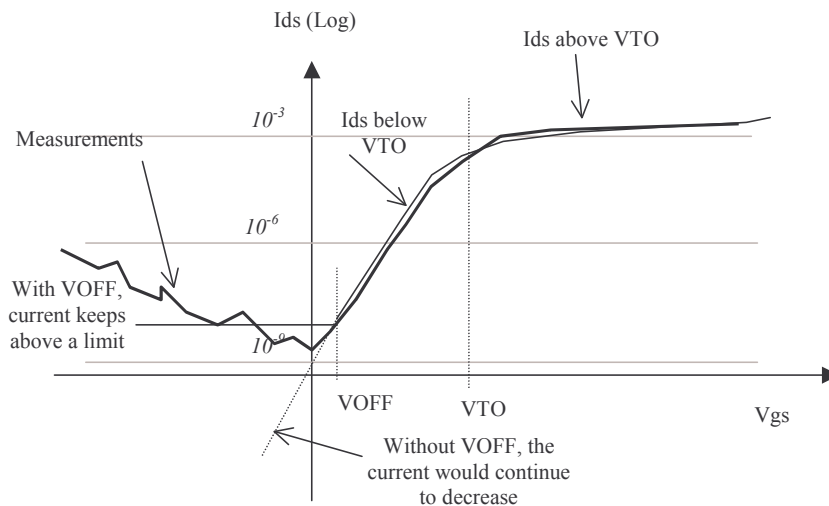


Figure 3-25: Illustration of the gate-induced drain leakage (GIDL) for negative V_{gs}

In reality, I_{ds} stops decreasing near zero V_{gs} , and then tends to increase with negative V_{gs} (Figure 3-25). This effect is called gate-induced drain leakage (GIDL). Consequently, the leakage current I_{off} can be

significant when V_{gs} is negative (Quite frequent in logic cells). The V_{OFF} parameter stops the I_{ds} at a certain value, a simplified version of the BSIM4 modeling of the so-called gate-induced leakage current (More info may be found in [Liu]).

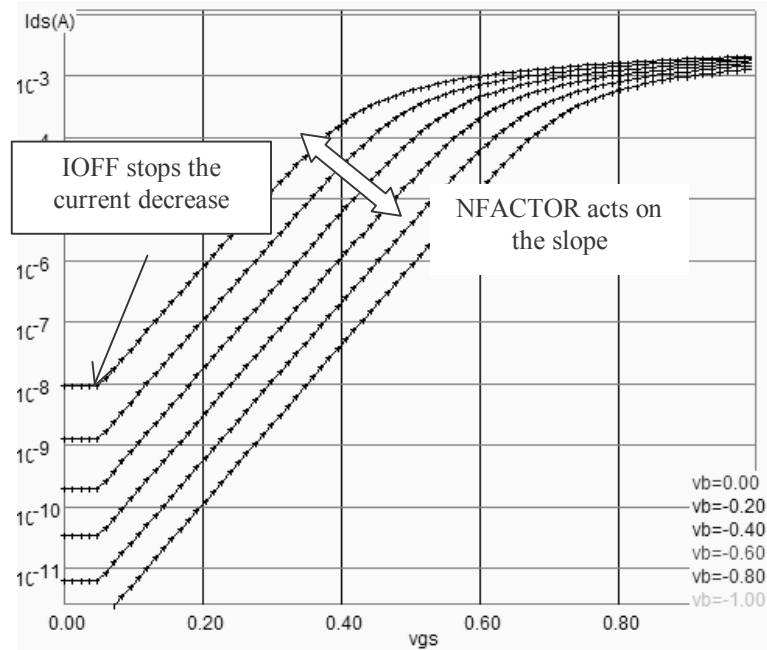


Figure 3-26: Illustration of the effects of IOFF and NFACTOR in sub-threshold mode

The parameter NFACTOR is usually close to 1, meaning that n is close from 2 (Equation 3-34). The effect on NFACTOR is illustrated in the display mode **Id. vs. Vg**, in logarithmic scale, as illustrated in figure 3-26.

$$E_{sat} = 2 \frac{V_{sat}}{\mu_{eff}} \quad (3-35)$$

$$V_{dsat} = E_{sat} \cdot L \frac{(V_{gsteff} + 2 \cdot v_t)}{(E_{sat} \cdot L + V_{gstEff} + 2 \cdot v_t)} \quad (3-36)$$

Again, V_{dsEff} is defined so as to smooth the evolution from V_{ds} to the saturation voltage V_{dsat} (Equation 3-37). The parameter $DELTA$ is fixed to 0.01. The effect of $DELTA$ is shown in figure 3-27. With a small value of $DELTA$ (0.001 for example), the transition between linear and saturated region leads to a discontinuity. Experimental measurements show a gradual transition, that is well approximated when $DELTA=0.01$. A higher value of $DELTA$ would lead to an I_{ds} curve significantly lower than measurements.

$$V_{dseff} = V_{dssat} - 0.5(V_{dsat} - V_{ds} - \delta + \sqrt{(V_{dsat} - V_{ds} - \delta)^2 + 4\delta \cdot V_{dsat}}) \quad (3-37)$$

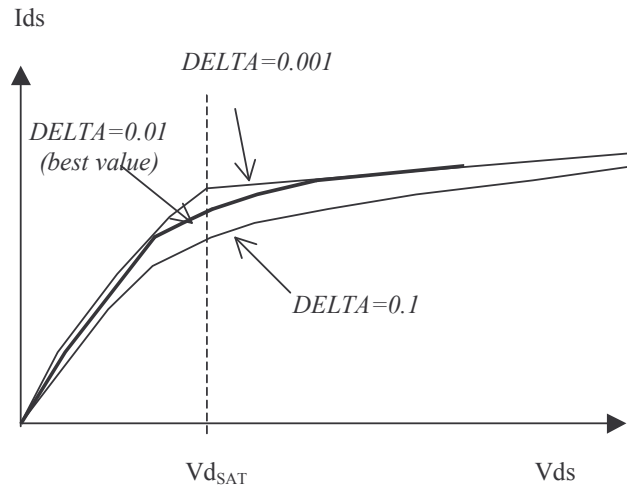


Figure 3-27: The smoothing function between linear and saturated regions can be modulated by DELTA. In Microwind2, DELTA is fixed to 0.01.

Current Ids

The current Ids is computed using one single equation, as described below.

$$Ids0 = \frac{W_{eff}}{L_{eff}} \mu_{eff} \frac{\epsilon_0 \epsilon_r}{TOXE} V_{gsteff} \left(1 - \frac{A_{bulk} V_{dseff}}{(2V_{gsteff} + 4.vt)} \right) \frac{V_{dseff}}{\left(1 + \frac{V_{dseff}}{\epsilon_{sat} L_{eff}} \right)} \tag{3-38}$$

In our implementation of BSIM4 in Microwind, the parameter *Abulk* is fixed to 1. The final current *Ids* used in analog simulation is computed by equation 3-39:

$$Ids = Ids0 \left(1 + \frac{(V_{ds} - V_{dseff})}{V_{asche}} \right) \left(1 + \frac{1}{C_{clm}} \ln \left(\frac{V_{ASAT} + V_{ACLM}}{V_{ASAT}} \right) \right) \tag{3-39}$$

Two new terms appear after *Ids0*. The second term of the current equation accounts for impact ionization. It corresponds to a parasitic current at very high *Vds*, created by hot electrons and generating supplementary pairs or electrons and holes, when hitting the drain region after acquiring a high energy level inside the device channel. The parameter *Vasche* is a voltage below which the impact ionization becomes significant. If *Vasche* is large, *Ids* is almost equal to *Ids0*, meaning that there is no impact ionization effect. If *Vasche* is small, the shape of *Ids* is changed for high *Vds*, as illustrated in figure 3-28.

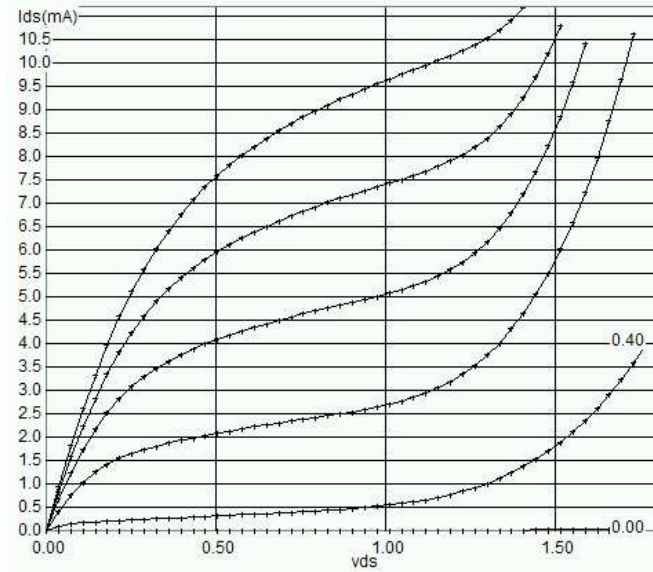


Figure 3-28: Effect of impact ionization at large V_{ds} ($W=10\mu m, L=0.12\mu m$).

Two parameters affect the shape of the ionization current : PSCBE1 and PSCBE2. The first parameter can be changed interactively on the screen. The voltage V_{asbe} is determined thanks to the following equations:

$$V_{asbe} = \frac{L_{eff}}{PSCBE2} \exp\left(PSCBE1 \frac{litl}{(V_{ds} - V_{dseff})}\right) \tag{3-40}$$

with

$$Litl = \sqrt{XJ \frac{\epsilon_{rsi}}{\epsilon_{rsiO2}} TOXE} \tag{3-41}$$

XJ is the source/drain junction depth, around $0.1\mu m$ ($10^{-7}m$)

$TOXE$ is the oxide thickness, in m (Around 3nm in $0.12\mu m$)

ϵ_{rsi} = relative permittivity of silicon (11.7)

ϵ_{rsiO2} = relative permittivity of silicon oxide (3.9)

The third term of equation 3-39 accounts for the channel length modulation. An illustration of this phenomenon is provided in figure 3-29. It represents the I_{ds} increase with large V_{ds} . Graphically, V_{ACLM} is equivalent to an Early voltage, i.e. the value for which the I_{ds} slope would cross the horizontal axis for negative V_{ds} . For long channel devices ($L=1\mu m$ for example), the effect of channel length modulation effect is small, so V_{ACLM} has a very high value (10V). For very short channels ($0.12\mu m$ in the case of figure 3-30), a significant channel length modulation effect is observed, and V_{ACLM} is small.

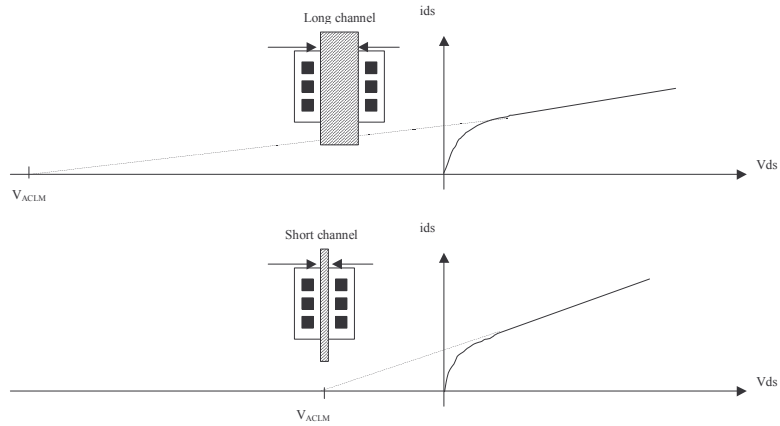


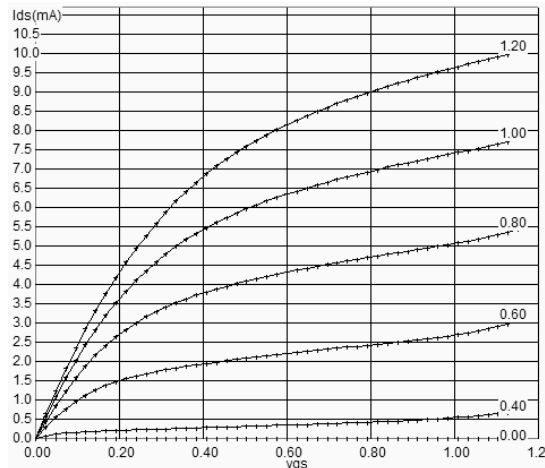
Figure 3-29: The channel length modulation is significant for short channel devices, and corresponds to the I_{ds} increase at high V_{ds} .

Only one new parameter, PCLM, is introduced in the equations. The parameters V_{ASAT} and V_{ACLM} are detailed below. The original equations from BSIM4 have been significantly simplified, and some fitting parameters have been ignored. See [Liu] for a description and relevant comments about the original equations.

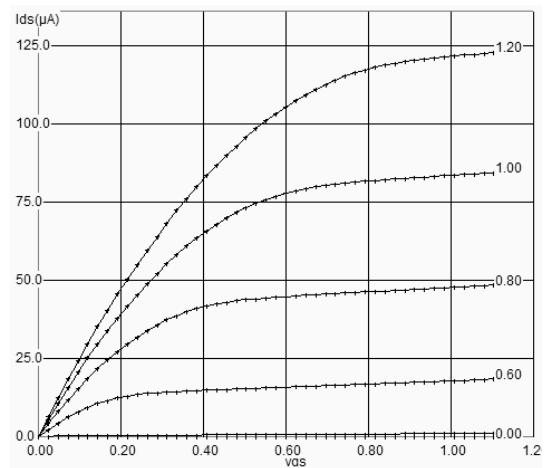
$$C_{clm} = \frac{1}{PCLM \cdot litl} \left(I_{eff} + \frac{V_{dsat}}{\epsilon_{sat}} \right) \tag{3-42}$$

$$V_{ACLM} = C_{clm} (V_{ds} - V_{dseff}) \tag{3-43}$$

$$V_{ASAT} = (\epsilon_{sat} \cdot I_{eff} + V_{DSSat}) \left(1 - \frac{A_{bulk} V_{dsat}}{2(V_{gsteff} + 2Vt)} \right) \tag{3-44}$$



(a) $L=0.12\mu m$, strong increase of I_{ds} with V_{ds}



(b) $L=1\mu m$ small increase of I_{ds} with V_{ds}

Figure 3-30: The channel length modulation effect is significant for short channel devices in $0.12\mu m$ technology

Temperature Effects

Three main parameters are concerned by the sensitivity to temperature: the threshold voltage V_{T0} , the mobility U_0 and the slope in sub-threshold mode. Both V_{T0} and U_0 decrease when the temperature increases. The modeling of the temperature effect in BSIM4 is as follows. In Microwind2, T_{NOM} is fixed to 300°K, equivalent to 27°C. U_{TE} is negative, and set to -1.8 in 0.12µm CMOS technology, while $KT1$ is set to -0.06 by default.

$$U_0 = U_{0(T=27)} \left(\frac{T + 273}{T_{NOM}} \right)^{U_{TE}} \tag{3-45}$$

$$V_T = V_{T0(T=27)} + KT1 \left(\frac{T + 273}{T_{NOM}} - 1 \right) \tag{3-46}$$

A higher temperature leads to a reduced mobility, as U_{TE} is negative. Consequently, at a higher temperature, the current I_{ds} is lowered. This trend is clearly illustrated in figure 3-31. The reduction of the maximum current is 40% between -30°C and 100°C.

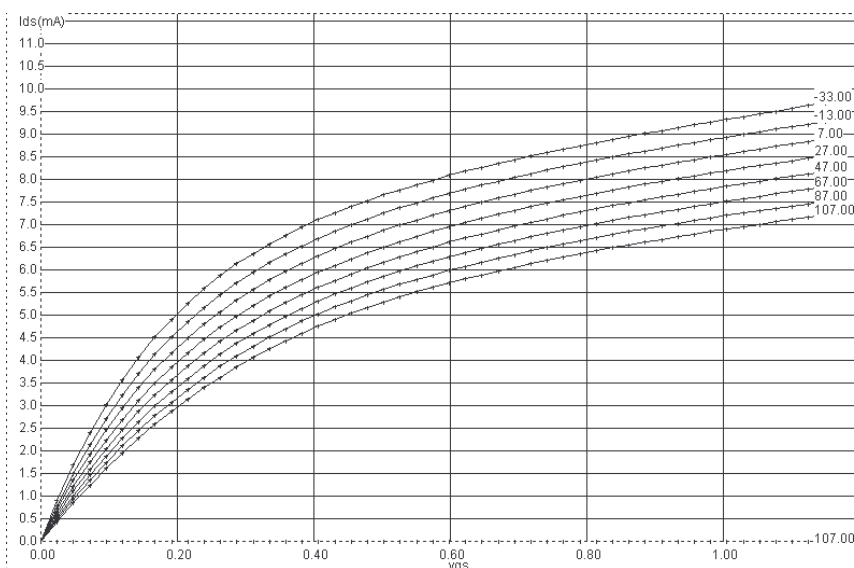


Figure 3-31: The effect of temperature on the peak I_{ds} current, showing a degradation of current with rising temperature

For a short channel n-channel MOS device ($L=0.12\mu\text{m}$), the result of the parametric analysis illustrates the same trend (Figure 3-33).The parametric analysis is conducted as follows: the layout **MosTemperature.MSK** is loaded first. The MOS is polarized with a gate always on, the drain at VSS, and the source at VDD. The parametric analysis is launched. In the new window, select the temperature (Upper menu) and the maximum current (Lower menu). We observe in figure 3-33 a significant decrease of the I_{on} current with the temperature.

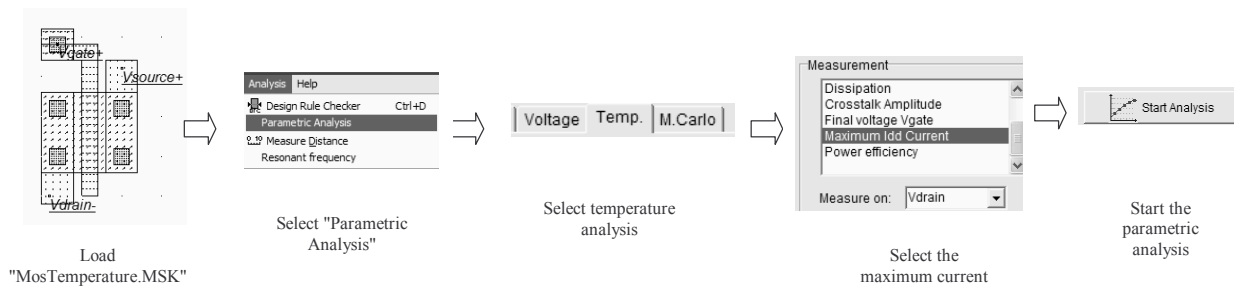


Figure 3-32: Configuring Microwind to display the variations of I_{ds} vs. temperature

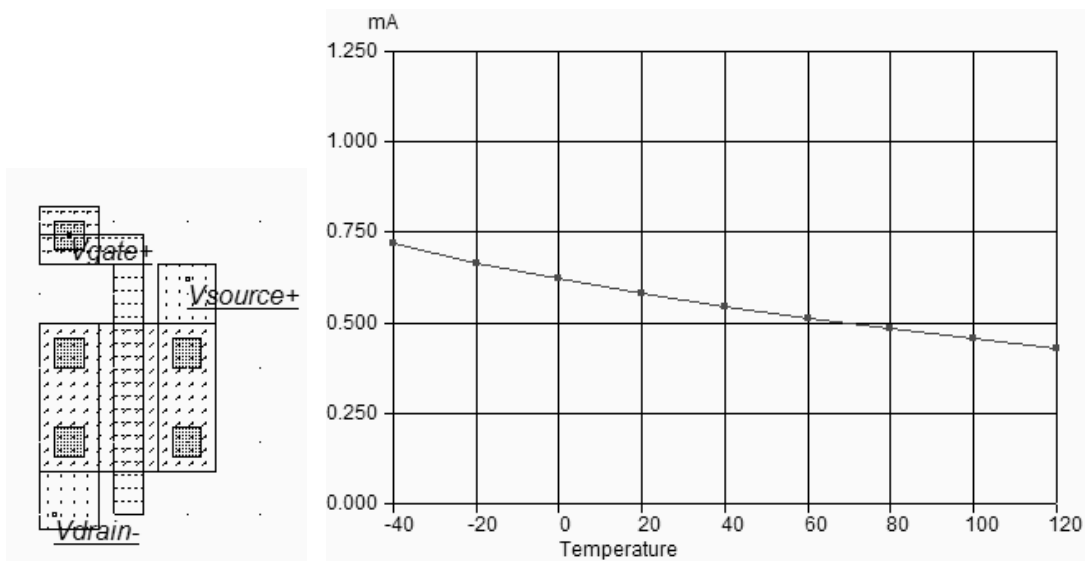


Figure 3-33: The parametric analysis reveals an important decrease of the maximum current I_{ds} with temperature (MosTemperature.MSK)

Meanwhile, in an opposite trend, the threshold voltage is decreased, as K_{T1} is negative (Figure 3-34). Therefore, there exists a remarkable operating point where the I_{ds} current is almost constant and independent of temperature variation. In $0.12\mu\text{m}$ CMOS, the V_{ds} voltage with zero temperature coefficient (ZTC) is around 0.9V, as shown in figure 3-34.

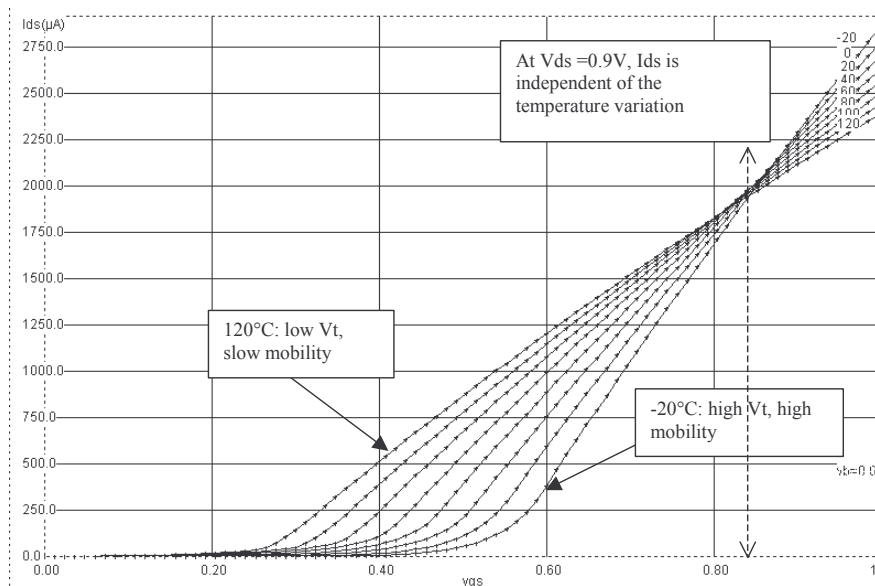


Figure 3-34: The effect of temperature on the I_{ds} current, showing a zero temperature coefficient (ZTC) operating point

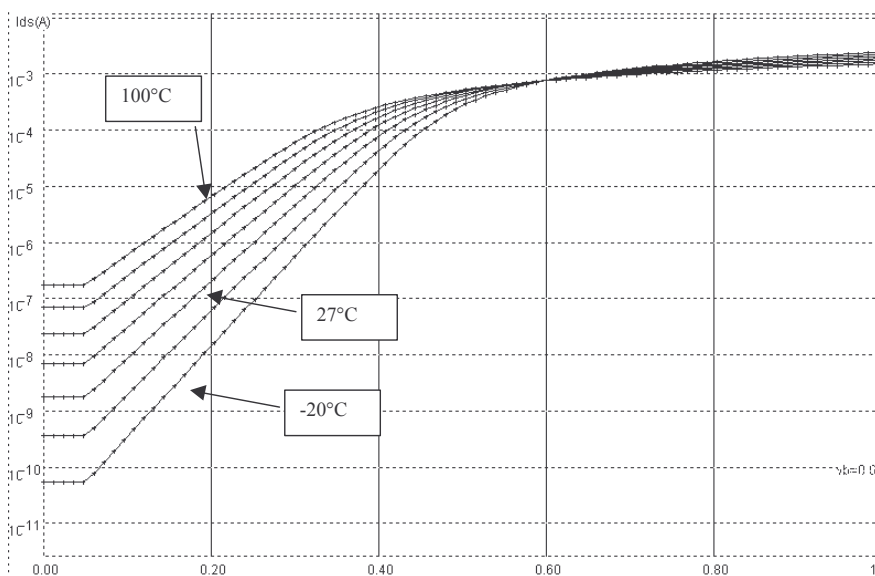


Figure 3-35 The effect of temperature on the MOS characteristics.

In the sub-threshold region, the impact of temperature is extremely important, as demonstrated in figure 3-35. At low temperature the current I_{ds} decreased rapidly down to 10nA, corresponding to a small off leakage current. In contrast, at high temperature, not only the threshold voltage is reduced but the sub-threshold slope is flattened, which means an exponential increase of the I_{off} leakage current (figure 3-35).

Parameter	Description	NMOS value in 0.12 μ m	NMOS value in 0.12 μ m	Name in RUL file
DVT0	First coefficient of short-channel effect on threshold voltage	2.2	2.2	B4D0VT
DVT1	Second coefficient of short-channel effect on V_{th}	0.53	0.53	B4D1VT
ETA0	Drain induced barrier lowering coefficient	0.08	0.08	B4ETA0
LINT	Channel-length offset parameter	0.01 $^{\circ}$ -6 μ m	0.01 $^{\circ}$ -6 μ m	B4LINT
LPE0	Lateral non-uniform doping parameter at $V_{bs} = 0$	2.3 $^{\circ}$ -10	2.3 $^{\circ}$ -10	B4LPE
NFACTOR	Sub-threshold turn-on swing factor. Controls the exponential increase of current with V_{gs} .	1	1	B4NFACTOR
PSCBE1	First substrate current induced body-effect mobility reduction	4.24e8 V/m	4.24e8 V/m	B4PSCBE1
PSCBE2	Second substrate current induced body-effect mobility reduction	4.24e8 V/m	4.24e8 V/m	B4PSCBE2
K1	First-order body bias coefficient	0.45 V $^{1/2}$	0.45 V $^{1/2}$	B4K1
K2	Second-order body bias coefficient	0.1	0.1	B4K2
KT1	Temperature coefficient of the threshold voltage.	-0.06V	-0.06V	B4KT1
NDEP	Channel doping concentration	1.7 $^{\circ}$ 17 cm $^{-3}$	1.7 $^{\circ}$ 17 cm $^{-3}$	B4NDEP
PCLM	Parameter for channel length modulation	1.2	1.2	B4PCLM
TOX	Gate oxide thickness	100nm	100nm	B4TOX
UA	Coefficient of first-order mobility degradation due to vertical field	11.0e-15 m/V	11.0e-15 m/V	B4UA
UC	Coefficient of mobility degradation due to body-bias effect	-0.04650e-15 V $^{-1}$	-0.04650e-15 V $^{-1}$	B4UC
U0	Low-field mobility	0.060 m 2 /Vs	0.025 m 2 /Vs	B4U0
UTE	Temperature coefficient for the zero-field mobility U_0 .	-1.8	-1.8	B4UTE
VFB	Flat-band voltage	-0.9	-0.9	B4VFB
VOFF	Offset voltage in subthreshold region.	-0.08V	-0.08V	B4VOFF
VSAT	Saturation velocity	8.0e4 m/s	8.0e4 m/s	B4VSAT
VTHO	Long channel threshold voltage at $V_{bs} = 0V$	0.3V	0.3V	B4VTHO
WINT	Channel-width offset parameter	0.01 $^{\circ}$ -6 μ m	0.01 $^{\circ}$ -6 μ m	B4WINT
XJ	Source/Drain junction depth	1.5 $^{\circ}$ -7m	1.5 $^{\circ}$ -7m	B4XJ

Table 3-4 List of user-accessible parameters in the BSIM4 implementation in Microwind.

5. Specific MOS devices

New kinds of MOS devices have been introduced in deep submicron technologies, starting the 0.18 μ m CMOS process generation. These MOS devices have specific characteristics which are described in this section.

Low leakage MOS

The main objective of the low leakage MOS is to reduce the I_{off} current significantly, that is the small current that flows between drain and source with a zero gate voltage. The price to pay is a reduced I_{on} current. The designer has the possibility to use high speed MOS devices, which have high I_{off} leakages but large I_{on} drive currents. The symbols of the low leakage MOS and the high speed MOS are given in figure 3-36.

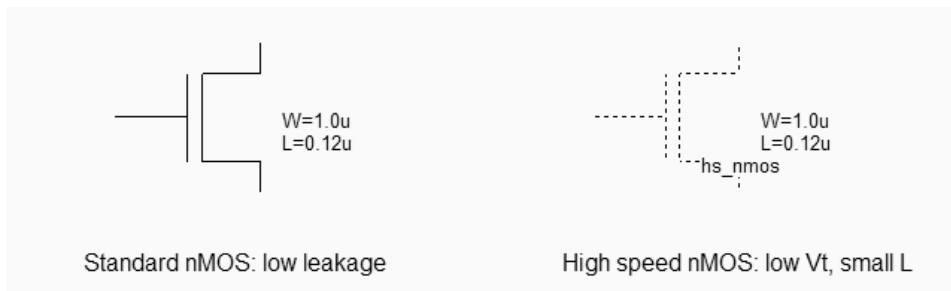


Figure 3-36: The low leakage MOS symbol (left) and the high speed MOS symbol (right) (MosOptions.SCH)

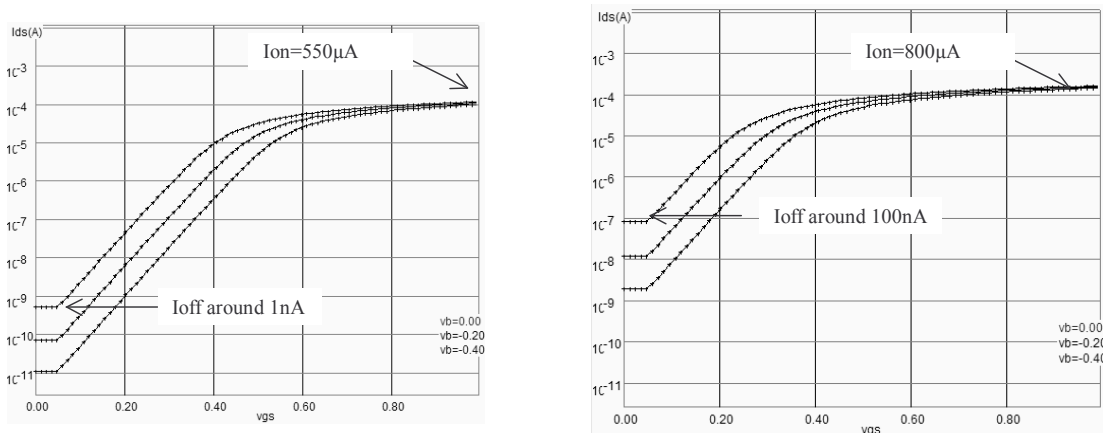


Fig. 3-37: The low leakage MOS offers a low I_{off} current (1nA) but a reduced I_{on} current (550 μ A) as compared to the high speed MOS

In figure 3-37, the low leakage MOS device (left side) has an I_{off} current reduced nearly by a factor 100, thanks to a higher threshold voltage (0.4V rather than 0.3V) and larger effective channel length (120nm) compared to the high speed MOS (100nm, see figure 3-30). By default, the MOS device is in low leakage option, to encourage low power design. The I_{on} difference is around 30%. This means that an high speed MOS device is 30% faster than the low leakage MOS. Its use is justified in circuits where speed is critical.

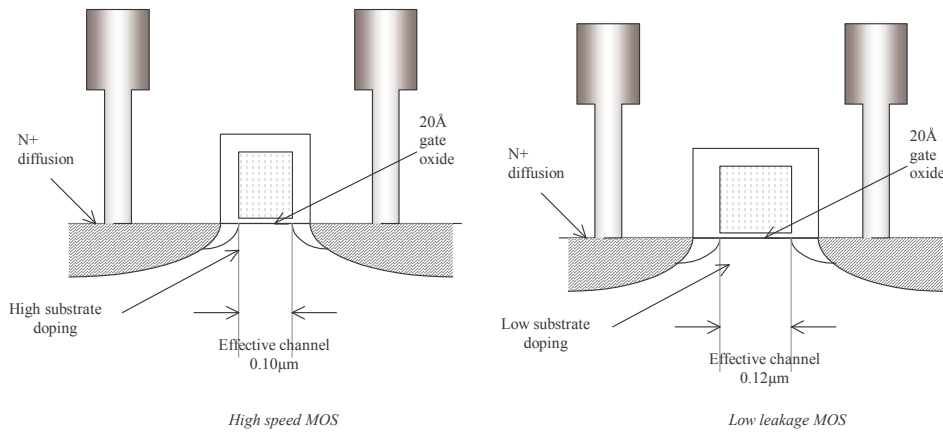


Fig. 3-38: Process section of the high speed (left) and low leakage (right) MOS devices

High speed MOS devices may be found in clock trees, data bus interfaces, central processing units, while low leakage MOS are used whenever possible, for all nodes where a maximum switching speed is not mandatory.

Mos options in Microwind

A specific layer, called option layer, is used to configure the MOS device option. The layer is situated in the upper part of the palette of layers. The bird's view of the standard MOS is identical to the high speed MOS, except for the added option layer which surrounds the MOS device. The p-channel MOS device includes an option layer together with the n-well layer, as seen in figure 3-39.

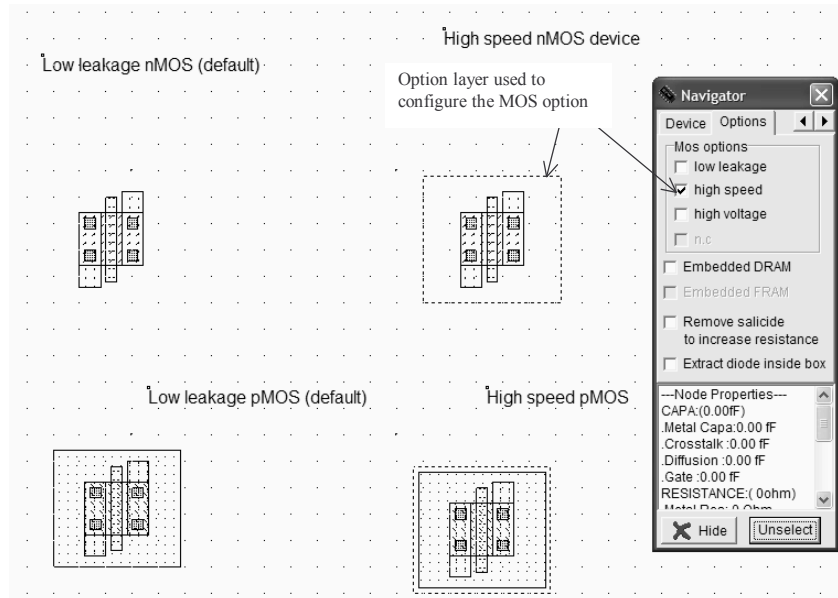


Fig. 3-39: High speed and Low leakage MOS layout. The only difference is the option layer configured for the low leakage option

An "Ultra-high speed" MOS has been introduced, together with the 90nm technology. This MOS device has a very narrow channel, nearly half of the technology, which increases significantly the I_{on} current at the price of a very high I_{off} parasitic leakage current (Figure 3-40).

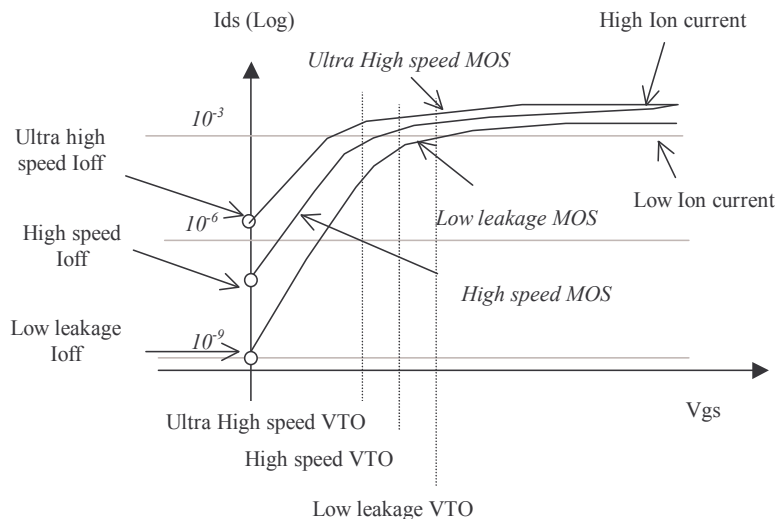


Fig. 3-40: Three types of MOS with different V_{TO} threshold voltage are available in 90nm technology.

High Voltage MOS

Integrated circuits with low voltage internal supply and high voltage I/O interface are getting common in deep sub-micron technology. The internal logic of the integrated circuit operates at very low voltage (Typically 1.0V in 0.12 μ m), while the I/O devices operate in standard voltages (2.5, 3.3 or 5V).

Figure 3-41 shows the evolution of the supply voltage with the technology generation. The internal supply voltage is continuously decreasing. For compatibility reasons, the chip interface is kept at standard voltages, depending on the target application. Consequently, the input/output structures work at high voltage thanks to specific MOS devices with thick oxide called "High Voltage MOS", while the internal devices work at low voltage for optimum performances.

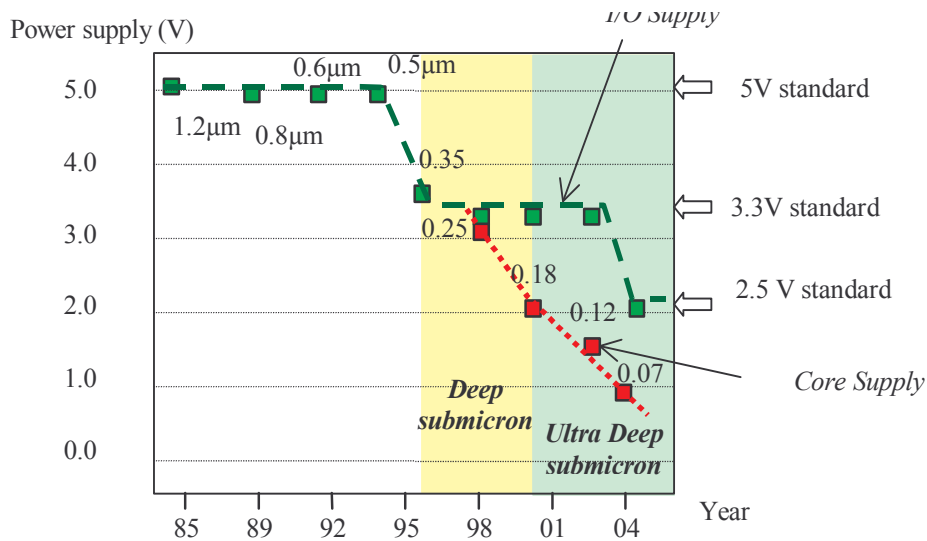


Fig. 3-41: The technology scale down leads to decreased core supply while keeping I/O interfacing compatible with 5V, 3.3V and 2.5V standards

For I/Os operating at high voltage, the high voltage MOS devices are commonly used. High-speed or low leakage devices would be dangerous to use because of their ultra-thin oxide: a 3V voltage applied to the gate of a core MOS device would damage the poly/substrate oxide. The high voltage MOS is built using a thick oxide, two to three times thicker than the low voltage MOS, to handle high voltages as required by the I/O interfaces (Figure 3-42). Furthermore, the length of the channel is 0.25µm minimum, that is twice the minimum length of core MOS. The cross-section of the three types of MOS (Low leakage, high speed and high voltage) is given in figure 3-43.

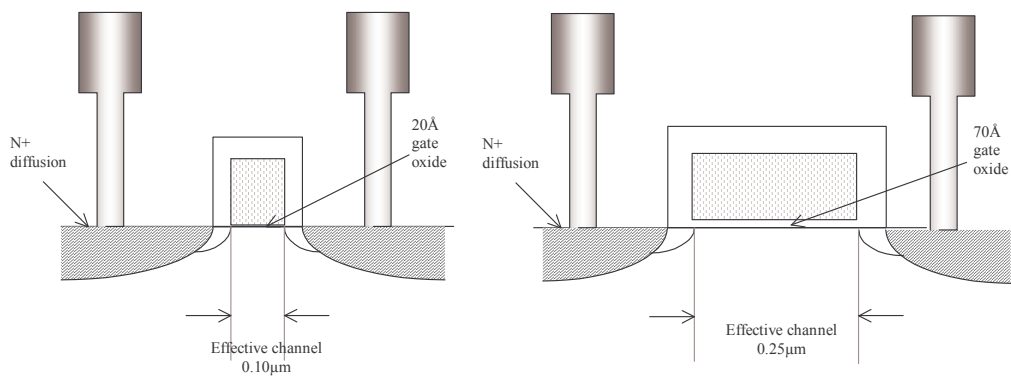


Fig. 3-42: Process section of the high speed and high voltage MOS devices

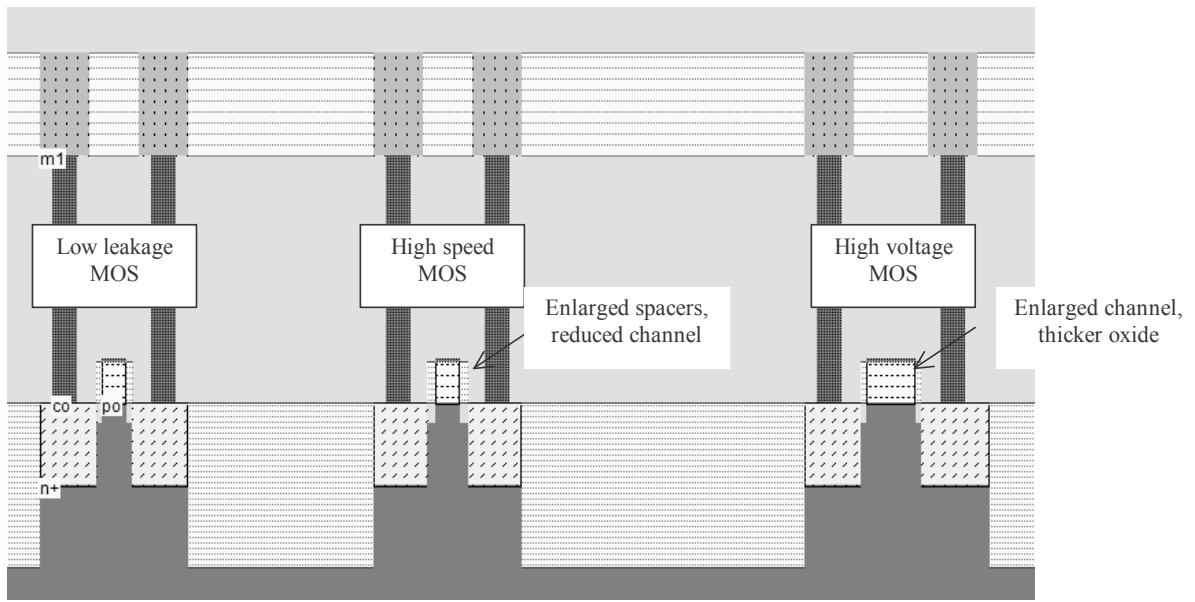


Fig. 3-43. The cross-section of the 3 n-channel MOS options: standard, high speed, and high voltage (lddExplain.MSK)

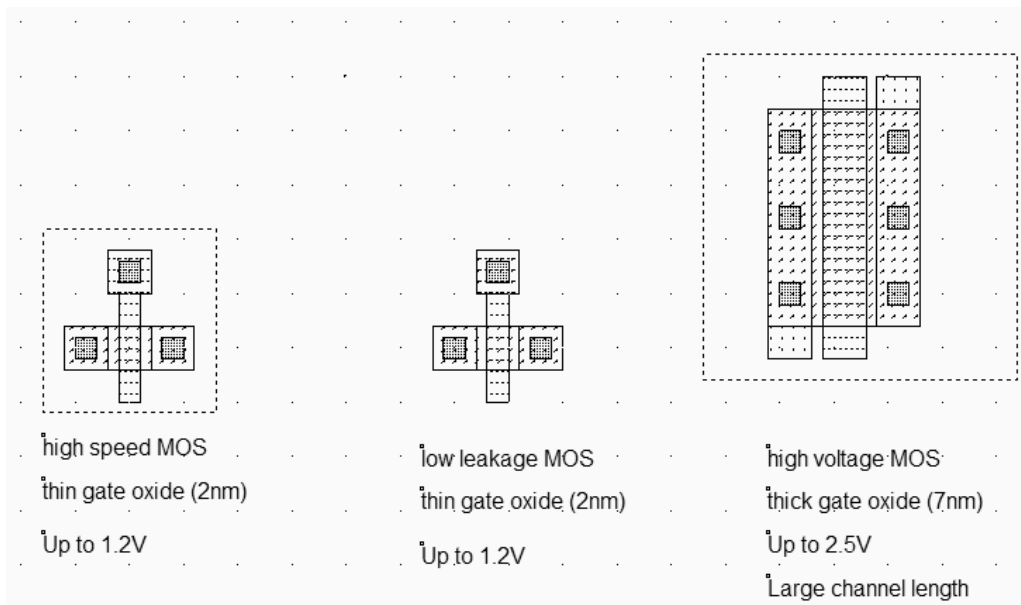


Fig. 3-44: High speed, low leakage and high voltage MOS (MosHighVoltage.MSK)

There is no difference between the high-speed MOS and the low leakage MOS from a layout point of view (Figure 3-44), expect the option layer for the high-speed option. The High voltage MOS has a significantly different layout, due to the enlarged channel length and width.

The I/V Characteristics of the high voltage MOS are plotted in figure 3-45, for V_{gs} and V_{ds} up to 2.5V. The channel length is $0.25\mu\text{m}$ and the channel width is $1.2\mu\text{m}$. Due to a large channel length, the current drive is less efficient.

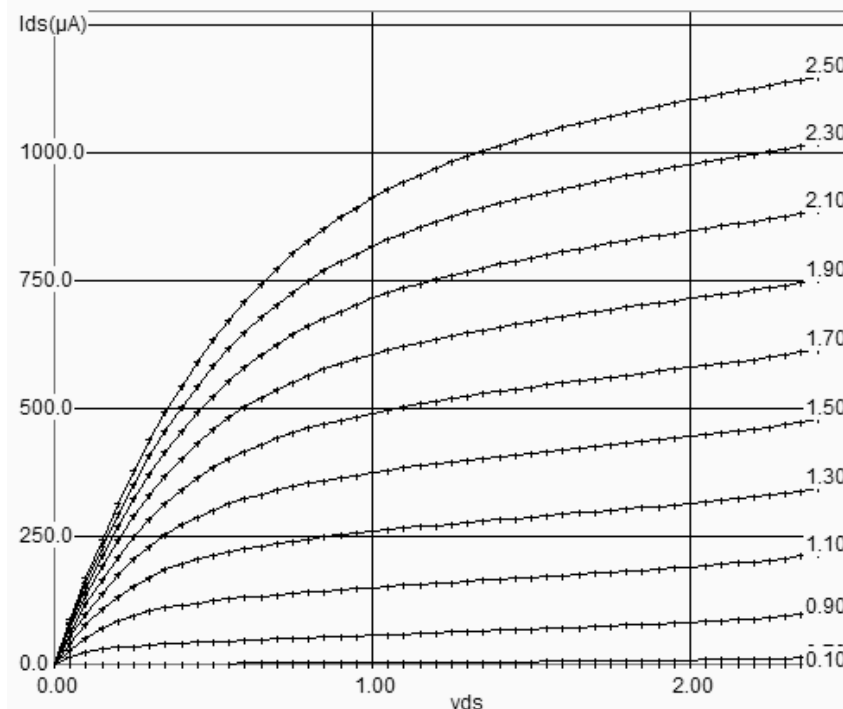


Fig. 3-45: I_{ds}/V_{ds} characteristics of the high voltage MOS.

There are two main reasons to keep a low-voltage supply for the core of the integrated circuit. The first one is low-power consumption, which is of key importance for integrated circuits used in cellular phones or any portable devices. Low supply strongly reduces power consumption by reducing the amplitude of signals, thus reducing the charge and discharge of each elementary node of the circuit. The equation 3-xxx gives an approximation of the power consumption. We deduce that even a small reduction of V_{dd} has a very positive impact on the reduction of the power consumption.

$$P = k \cdot C \cdot f \cdot V_{DD}^2 \quad (3-47)$$

where

P = power consumption (Watts)

K =technology factor, close to 0.5

C = total active capacitance of electrical nodes (F) (Not taking into account decoupling capacitance)

f =operational frequency of the integrated circuit (Hz)

V_{dd} = supply voltage (V)

Oxide Breakdown

The second reason for internal low voltage operation is the oxide breakdown. Increased switching performances have been achieved by a continuous reduction of the gate oxide thickness. In 0.12µm technology, the MOS device has an ultra thin gate oxide, around 0.002µm, that is 2nm or 20 Å. Knowing that the molecular distance of SiO2 oxide is around 2Å, 20 Å means 10 atoms. The oxide may be destroyed by a voltage higher than a maximum limit V_{crit} , called oxide breakdown voltage. A first order estimation is 0.1V/Å [Wang], which is expressed by equation 3-47.

$$V_{crit} = \frac{K}{tox} \quad (3-47)$$

With

K=breakdown coefficient (Close to 1 V.nm)

Tox = oxide thickness in nm

Vcrit=critical breakdown voltage (V)

Consequently, in 0.12µm, the breakdown voltage is around 2.0V, that is less than twice the nominal VDD (1.2V). An illustration of the breakdown voltage is proposed in figure 3-xxx. If we display the Id/Vd characteristics with Vg higher than VDD, (for example 2.5V instead of 1.2V), the oxide damage is represented by dotted lines (Here for Vg>2.0V). The MOS polarization should always be fixed in such a way that the gate voltage is lower than the breakdown voltage limit.

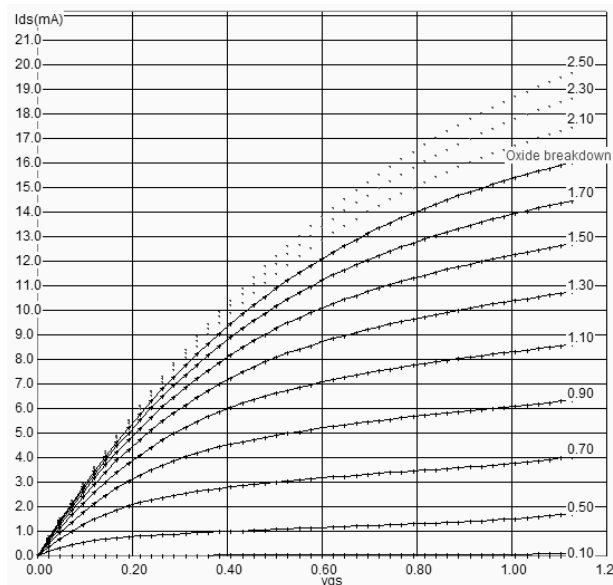


Fig. 3-46. Illustration of the breakdown voltage for a low leakage nMOS device, with a very high voltage applied on the gate

The oxide may be damaged by a 2V gate voltage. If the gate voltage is further increased, the physical destruction of the oxide may be observed, which usually results in a permanent conductive path between the gate and the source (Figure 3-47).

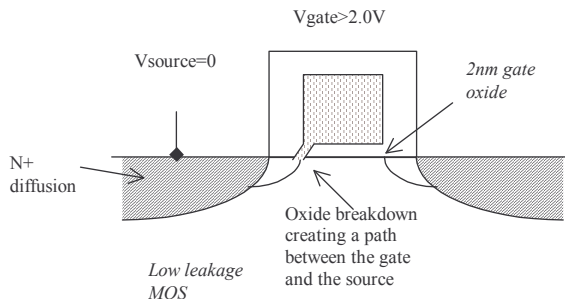


Fig. 3-47: oxide breakdown appears for gate voltage significantly higher than the nominal supply voltage

Microwind Configuration

A set of specific parameters are used for each MOS option to configure the BSIM4 and LEVEL3 models. The industrial approach usually consists in describing each MOS device in a completely separated set of model parameters. Consequently, MOS model cards may include several thousands of parameters. We are trying to be as practical and didactic as possible, at the cost of a poor matching between measured and simulated MOS characteristics. In table 3-5, the list of the main varying parameters includes the gate oxide, the effective channel length parameter, and the threshold voltage.

Parameter	Description	NMOS value in 0.12µm	NMOS value in 0.12µm	Name in RUL file
TOX	Gate oxide thickness (low leakage) (high speed) (high voltage)	20Å 20 70	20Å 20 70	B4TOX B4T2OX B4T3OX
LINT	Channel-length offset parameter (low leakage) (high speed) (high voltage)	0.0 nm 10 0.0	0.0 nm 10 0.0	B4LINT B4L2INT B4L3INT
VTHO	Long channel threshold voltage (low leakage) (high speed) (high voltage)	0.40 V 0.30 0.50	0.40 V 0.30 0.50	B4VTHO B4V2THO B4V3THO

Table 3-5: BSIM4 parameters variation depending on the MOS option

6. Process Variations

The simulated results should not be considered as absolute values. Due to unavoidable process variations during the hundreds of chemical steps for the fabrication of the integrated circuit, the MOS characteristics are never exactly identical from one device to another, and from one die to another. It is very common to measure 5% to 20% electrical difference within the same die, and up to 30% difference between separate dies. One varying parameter is the effective channel length. In figure 3-48, although both devices have been designed with a drawn 2 lambda, the result is a 0.11µm length for the MOS situated on the left side, and 0.13µm for the MOS situated on the right side.

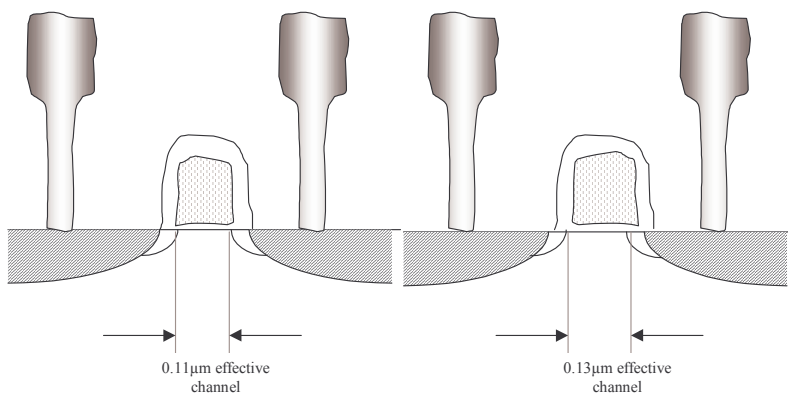


Fig. 3-48: The same MOS device may be fabricated with an important effective channel variation

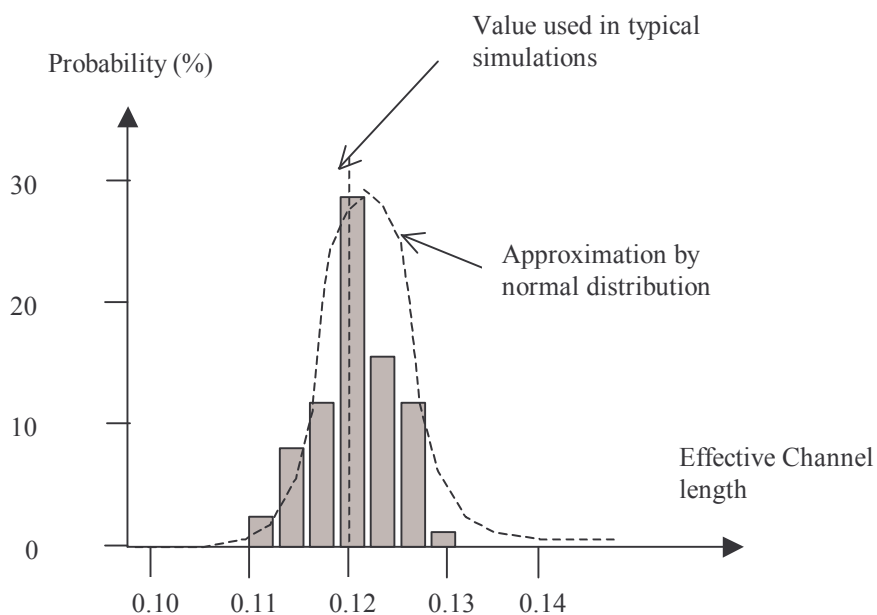


Fig. 3-49: The effective channel length may vary significantly with the process

If we cumulate several measurements on a wide number of devices, we can plot the probability of occurrence versus the measured effective length. The curve is usually a normal distribution with a center close to the default parameter given in the electrical rules (Figure 3-49).

Simulation with Microwind

The menu **Simulate** → **Simulation parameters** gives a simple access to minimum/typical/maximum parameter sets (Figure 3-50). The industrial approach usually consists in providing a separate set of model parameters for each case, which represents a huge amount of model parameters. In Microwind, the approach has consisted in altering two main parameters: the threshold voltage (20% variation) and the mobility (20% variation). All other parameters are supposed to be constant.

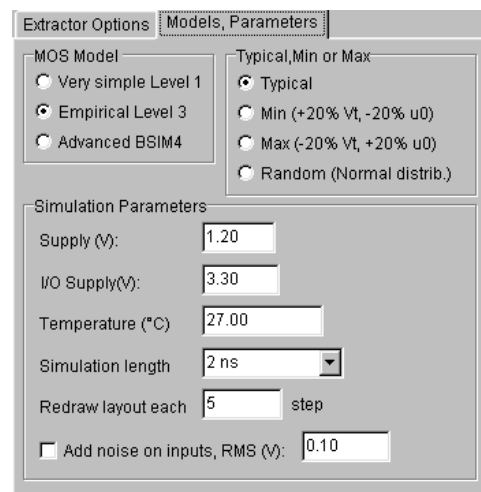


Fig. 3-50: Access to minimum, typical, maximum model parameters or Random simulation

A comparative simulation of the I_d/V_d curve in typical, maximum and minimum scenarios shows a very large variation of performances (Figure 3-51). The user may automatically switch from one parameter set to an other by a press of a key ("M" for maximum, "m" for minimum, "t" for typical).

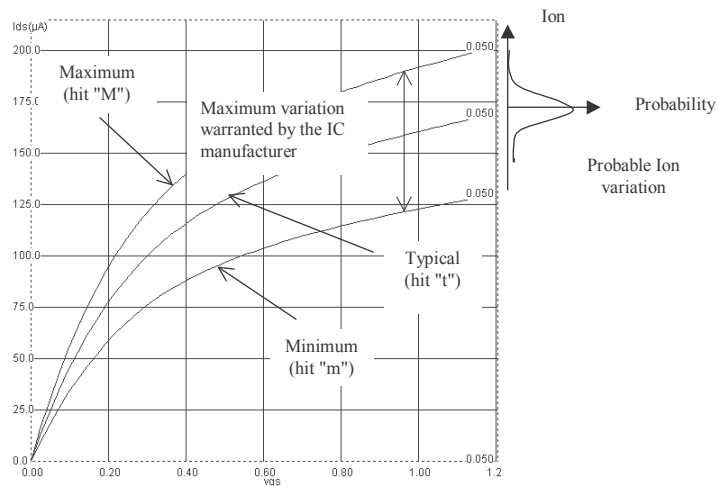


Fig. 3-51: The MOS Id/vd curve in Min, Typ, Max modes.

To superimpose the three curves, click the small brain icon (Enable Memory), and increase the **Step Vg** to 1.2 to draw only one curve for each mode. Notice the important variation between the minimum Ion and maximum Ion (From 125µA to 200µA). In reality, the MOS characteristics vary in a normal distribution around the typical case. Consequently, the Ion current of this MOS device is very likely to reach the typical value. The min/max simulation is very interesting to validate the design in extreme situations. The min/max simulation should also consider the temperature: the worst current is obtained at high temperature and with a minimum set of parameters, while the highest current is obtained at low temperature and with a maximum set of parameters.

7. Concluding remarks

The number of parameters required for various MOS models is reported in figure 3-52. It can be seen that the trend is to increase the number of parameters, in order to take into account various effects linked to the device scale down.

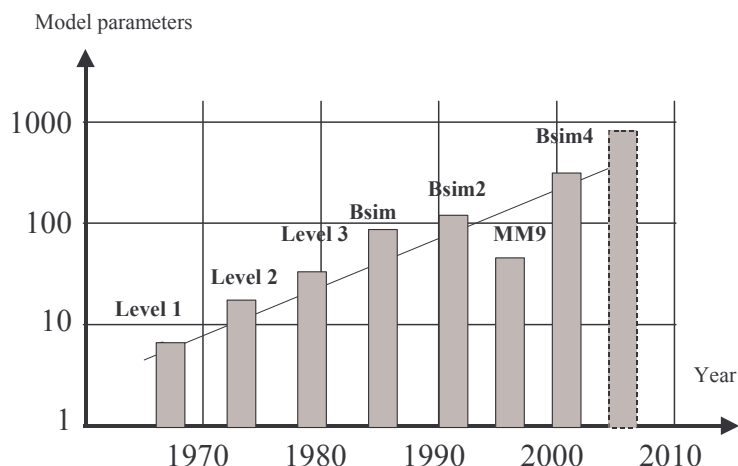


Fig. 3-52. Increased number of parameters in the MOS models

Even with advanced models, the resulting models may not fit well in all operating regions, for all device sizes. This is why the industrial approach for building model parameters is based on optimization mathematical algorithms. In deep submicron technology, the model parameters have a strong variation with the device size. For example the threshold voltage and mobility vary significantly with the device length, and the equations cannot always handle these dependencies properly. One solution is called binning. It consists in breaking the width-length space into several regions, as illustrated in figure 3-53. In each region, a specific set of model parameters is setup and optimized.

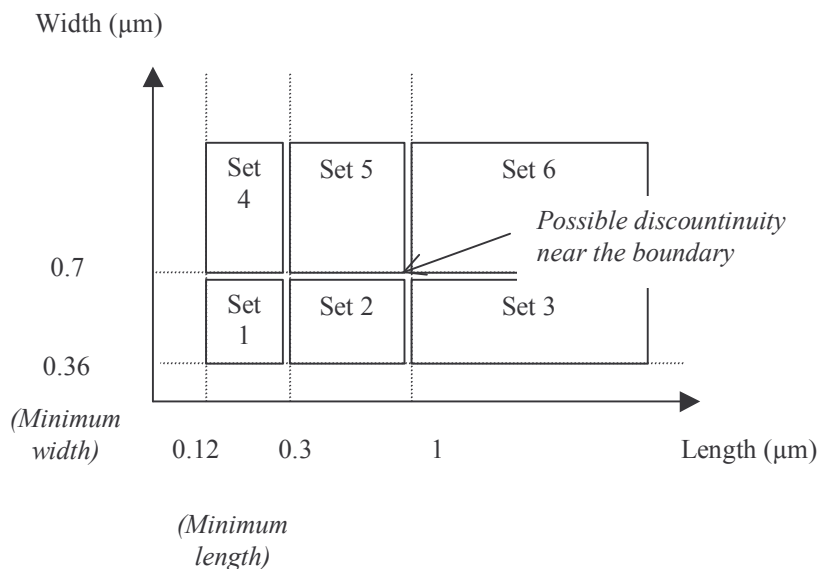


Figure 3-53: Using 6 sets of parameters to accurately cover the whole range of width and length

Binning severely complicates the process of parameters extraction. In the case of figure 3-xxx, 6 sets of parameters are required. Notice that set 1 covers small length and small width. Set n°2 covers a wider length

interval, while set $n^{\circ}3$ is valid for any length greater than $1\mu\text{m}$. This is because long length devices are easier to model than short length devices, where many second order effects appear. Binning is used in industry to increase the analog simulation accuracy, at the cost of several drawbacks: the simulation time cost due to model complexity, and discontinuities in the current prediction that may be observed at the boundary of two sets. These limitations are the fuel for constructing more complex models that fit well for the whole range of width and length. In the future, nano-scale technologies may require MOS models with up to 1000 parameters, requiring a degree of expertise never attained up to now.

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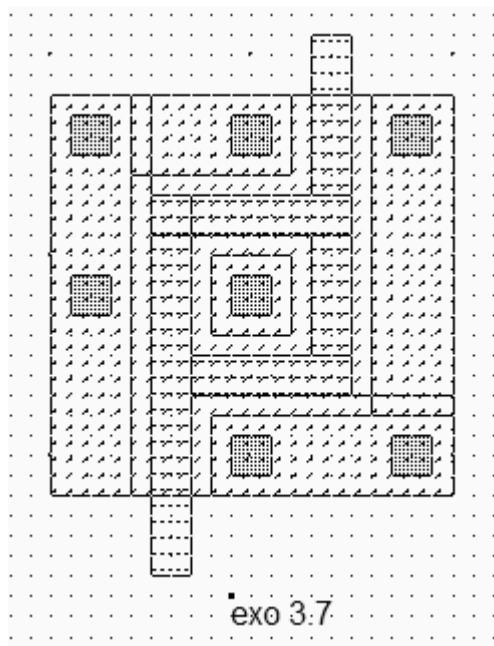
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EXERCISES

3.1 Configure Microwind in $0.35\mu\text{m}$ technology (File **cmos035.RUL**) using the command **File → Select Foundry**. Compare simulation and measurement in $0.35\mu\text{m}$ for a nMOS device, $W=10\mu\text{m}$, $L=0.4\mu\text{m}$ (File **Na10x0,4.MES**). Evaluate the mismatch between level 1, level 3 and BSIM4. In which domain is model 3 poorly fitted?

- 3.2 Configure Microwind in 0.18 μm technology (File **cmos018.RUL**). Compare simulation and measurement in 0.18 μm for a nMOS device, $W=4\mu\text{m}$, $L=0.2\mu\text{m}$, low leakage option (File **Nc4x0.2.mes**). Evaluate R_{on} , I_{on} , I_{off} , and V_t . Perform the same evaluation for the high speed MOS, same size (File **NcHS4x0.2.mes**). Perform the same evaluation for the high voltage MOS, same size (File **NcHV4x0.2.mes**).
- 3.3 In low power applications, the n-well can be connected to a voltage V_{well} different from VDD. This non usual polarization aims at modifying the threshold of the p-MOS transistor. Under which condition for V_{well} the threshold of the PMOS transistor (Low Leakage option) is decreased to 0.2V in 0.12 μm ?
- 3.4 Design a MOS device with $I_{on}=10\text{mA}$, minimum gate length in 0.12 μm . What is I_{off} ? How to obtain a MOS with $I_{on}=10\text{mA}$ but twice less I_{off} ?
- 3.5 Compare the value of $V_{GS_{T0}}$ (The value of V_{gs} for which I_{ds} is independent of temperature) between MOS options in 0.12 μm .
- 3.6 Show that four MOS devices (W_n, L_n) connected in parallel have approximately the same I_{on} than a single MOS device with a width equal to 4 W_n . What is the origin of the mismatch?
- 3.7 What is the channel size of the following MOS device? Does Microwind correctly extract the channel size of that device?



- 3.8 In the following picture of a 50nm MOS device, locate the gate, drain, and source, field oxide, gate oxide .

