9 Silicon On Insulator

1. Introduction

The use of Silicon-On-Insulator (SOI) technology is bringing interesting new possibilities compared to conventional bulk technology. This chapter highlights the extra performance and advantages offered by SOI, as well as the limiting parasitic effects. Performance improvements concern the power consumption and the commutation speed. In the best case, the SOI technology may cut the power consumption nearly by half, with speed improvements close to 30%. The speed improvement itself is equivalent to about two years of progress in bulk CMOS technology. The insulator material used in SOI is a buried SiO2 layer, illustrated in figure 9-1.

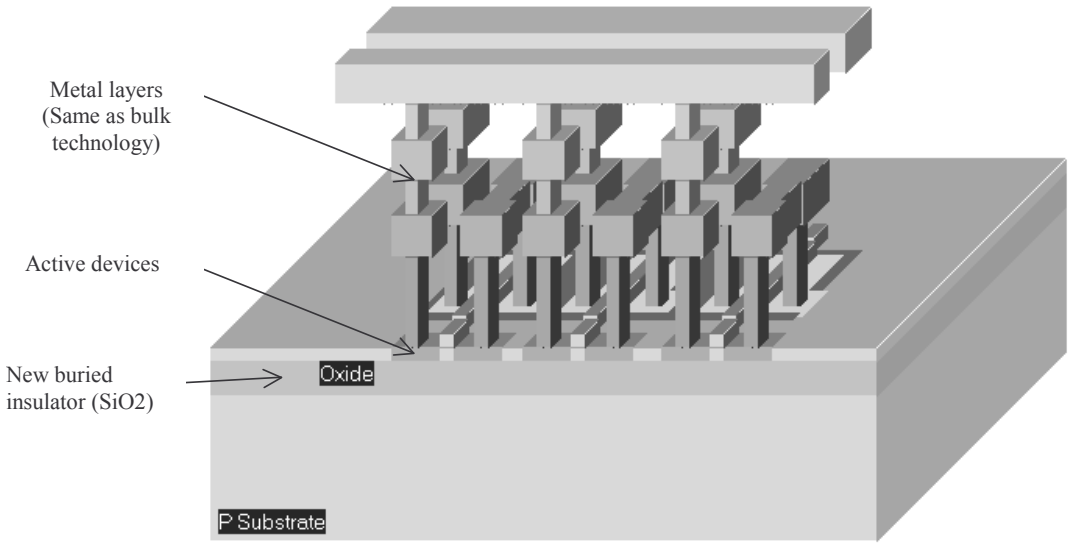


Figure 9-1 : 3D View of SOI ring inverter showing the SiO2 buried layer(inv3Soi.MSK)

In fact, the SOI technology has been available for more than 20 years, but its applications were mainly restricted to space and army due to very low sensitivity to radiation. The road to a commercial use of SOI still faces several issues: one is the cost of the substrate, which is 5 to 10 times the cost of a bulk wafer, an other is the need to train designers to specific design techniques and rules, as the behavior of a SOI MOS device differs slightly from the bulk MOS device. Although the MOS device fabrication is slightly modified, the fabrication of the metal interconnects is identical to that of the bulk CMOS process.

The SOI Substrate

SOI refers to placing a thin layer of silicon on top of a silicon oxide insulator, as illustrated in figure 9-2. The transistors are built on top of this thin layer of SOI. A 0.12µm SOI technology, namely **soi012.rul** is available in Microwind. It enables the comparative simulation with the corresponding bulk technology (**cmos012.rul**, the standard CMOS 0.12µm technology).

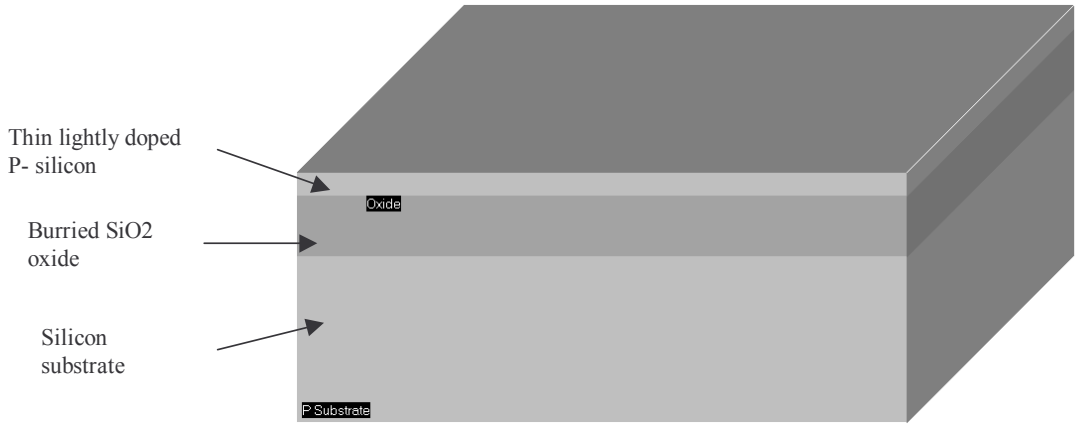


Figure 9-2 : 3D View of SOI ring inverter showing the SiO2 buried layer(inv3Soi.MSK)

The basic idea is that the SOI layer will reduce the parasitic junction capacitance of the switch, so it will operate faster. Every time the transistor is turned on, it must first charge all its internal capacitance before it can begin to switch. Among these parasitic capacitances are the junction capacitance *Csb* and *Cdb*, which are strongly reduced by the silicon dioxide, as described in the two-dimensional cross-section of figure 9-3. The thicker the SiO2 oxide, the smaller the parasitic capacitance. The typical insulator thickness is between 200 and 500nm. In the SOI CMOS 0.12µm technology provided with Microwind, the dielectric thickness is 300nm, and the silicon thickness on the top of the insulator is 150nm. As illustrated in the figure, the junction capacitance *Csb* and *Cdb* are significantly reduced, which is meant to speed up the switching of devices.

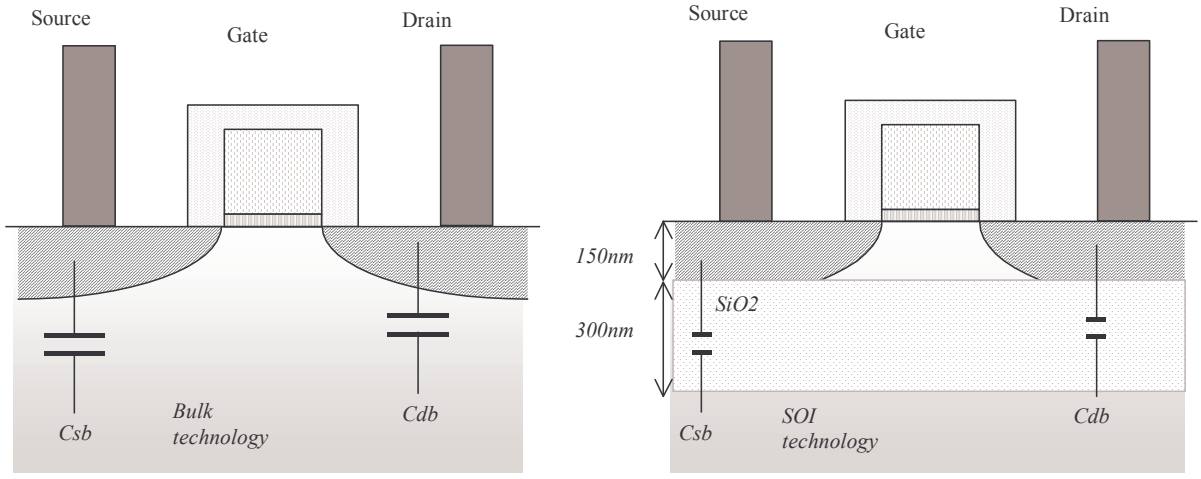
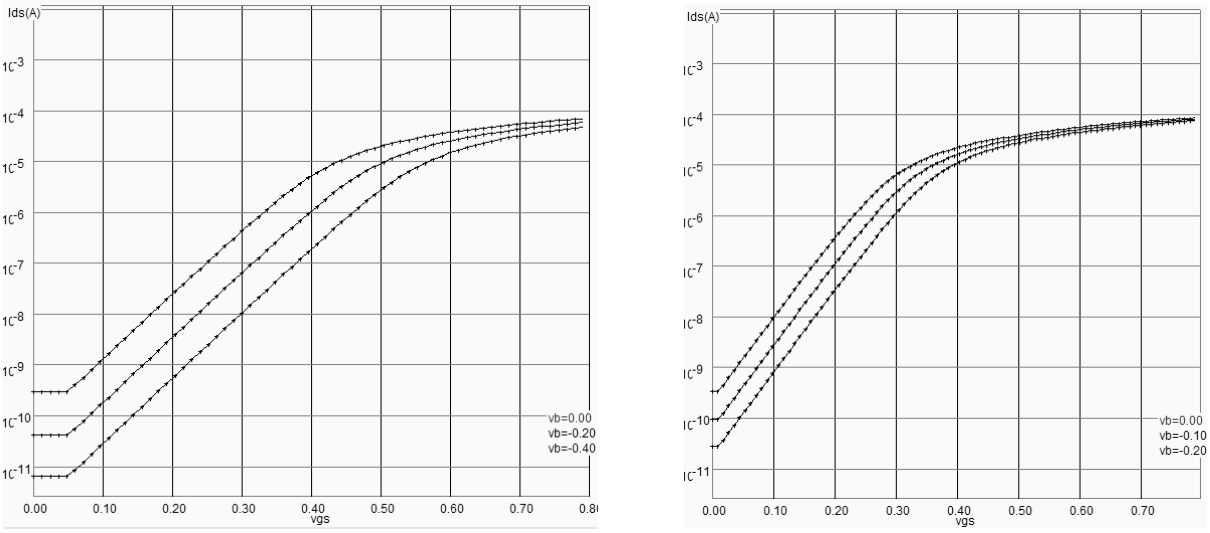


Figure 9-3: The junction capacitance between the source and bulk is almost eliminated in the case of SOI.

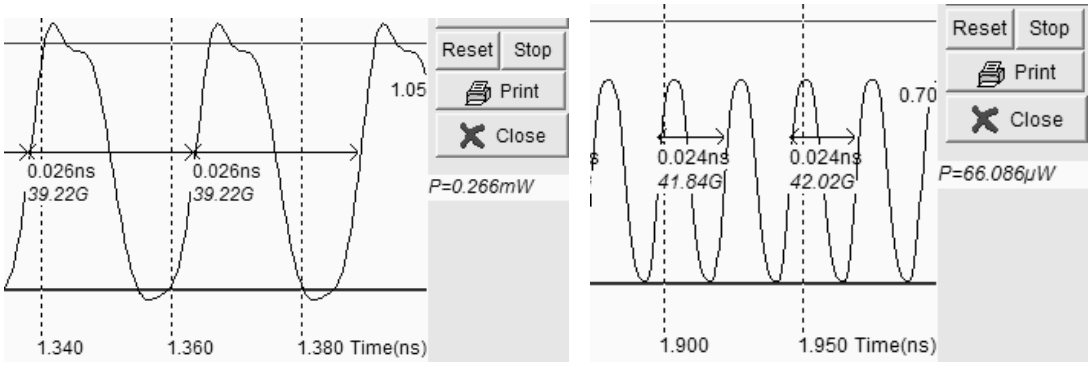
Low voltage Operation

An important feature of SOI devices is the steeper sub threshold slope due to a reduction of the substrate body effect. Typical sub threshold slope factors (NFACT in the BSIM4 menu) are close to 1.0 for SOI devices, as compared to 1.5 for bulk devices. For a given *Ioff* current, the SOI circuit may have a much smaller threshold voltage, which means that the circuit can operate at lower supply.



(a) Bulk MOS *(b) SOI MOS*

Figure 9-4: The steeper sub-threshold slope enables low voltage and low power operations.



(a) Bulk oscillator at 40GHz: 266µW *(b) SOI oscillator at 40GHz: 66µW*

Figure 9-5: The lower Ioff current and steeper sub-threshold slope enables low voltage and low power operations.

Recall that the power is proportional to the total circuit capacitor and the square of the supply voltage. This means that SOI circuits are very good candidates for low power operations as the parasitic capacitance is reduced and the supply voltage can be lowered. Considering the ring oscillator with three inverters, we obtain a 42GHz oscillation at a supply voltage of 0.7V in SOI technology, rather than 1.2V in bulk technology (Figure 9-5). The power gain is approaching a factor of 4.

Furthermore, the lower sub threshold combined with a stepper slope is of key interest for analog circuits, which can provide the same functionality and approximately the same bandwidth performances, with a lower power consumption.

Increased density

One important feature of the SOI technology concerns the CMOS cell density increase thanks to relaxed design rule constraints between N+ and P+ diffusions. In CMOS bulk technology, the n-channel device is separated from the p-channel device by at least 12 lambda. In SOI technology, the design rule drops to only 2 lambda, as shown in figure 9-6.

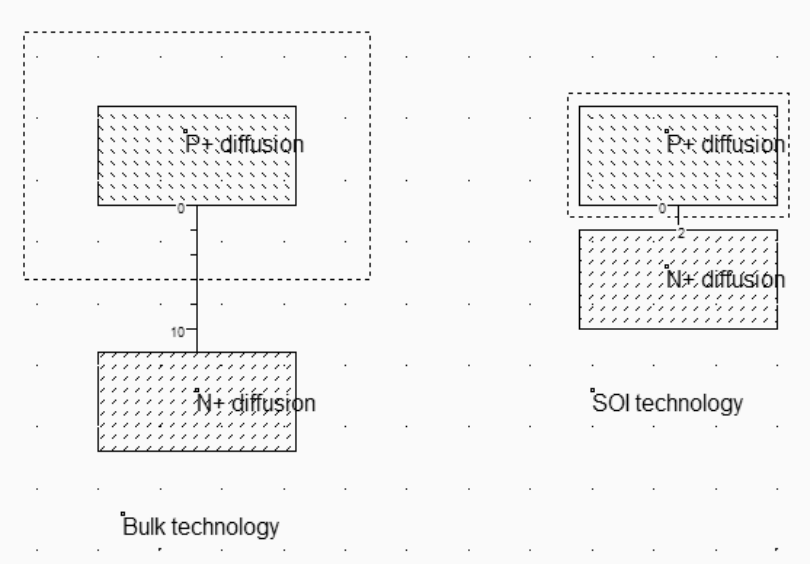


Figure 9-6: The increased density due to relaxed design rules between N+ and P+ diffusions (SOIDiffusion.MSK)

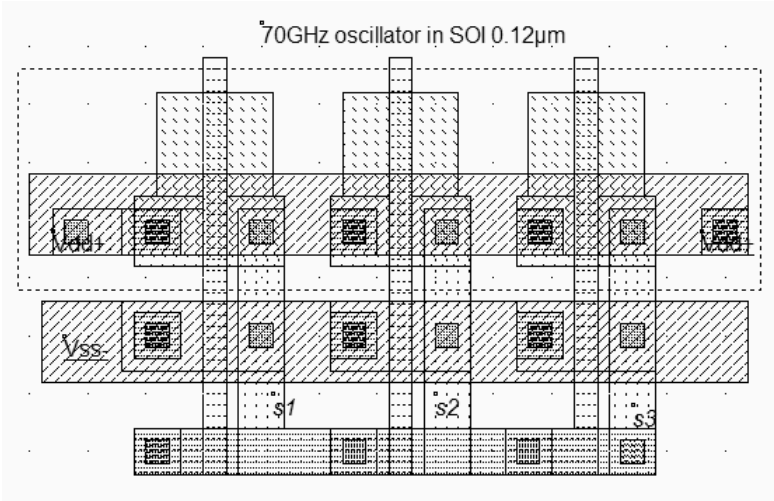
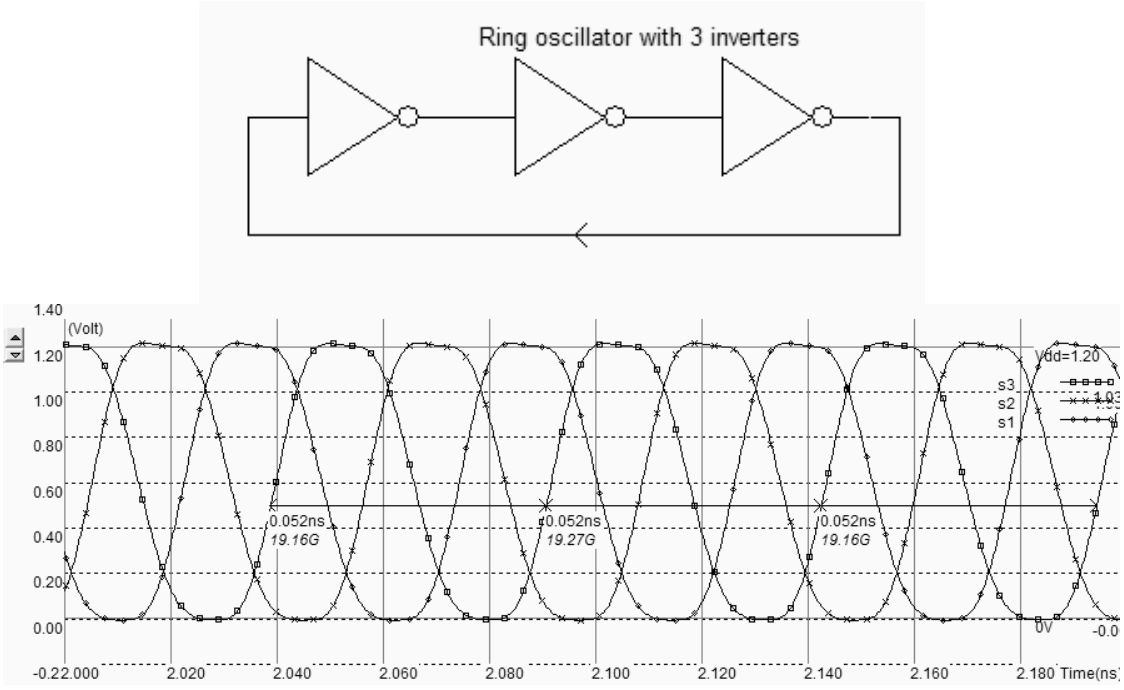


Figure 9-7: The ring oscillator in SOI technology (Inv3SOI.MSK)

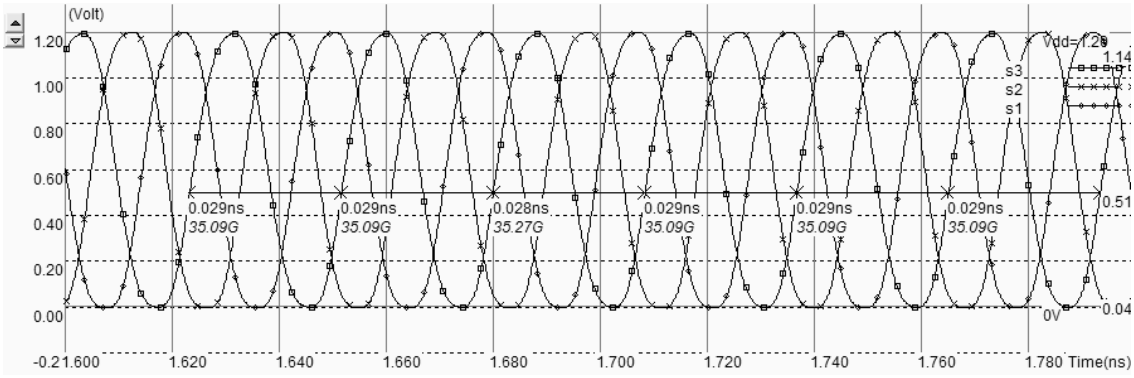
Consequently, the layout implementation of a CMOS cell is more compact as the nMOS and pMOS devices almost touch each other. As an example, the 3-inverter ring oscillator in SOI technology is 20% more compact than the bulk version (Figure 9-7), for an identical sizing of nMOS and pMOS devices.

Increased Operating Frequency

The comparison between the SOI ring inverter and the bulk ring inverter is given in figure 9-8. We observe a very significant gain in terms of speed, nearly 80% in this case. In bulk technology, the 3-inverter oscillator (Inv3.MSK) is operating near 19GHz, when using the model BSIM4. In SOI technology, the same inverter oscillates (Inv3Soi.MSK) around 35GHz.



(a) Bulk technology



(b) SOI technology

Figure 9-8: The simulation of the ring oscillator in bulk and SOI technologies (Inv3.MSK, Inv3SOI.MSK)

The very important frequency increase observed in figure 9-8 mainly finds its origin in the decreased parasitic capacitance of the drain junctions of the MOS devices. As no long interconnect was needed in this design, the reduction of capacitance has a very clear impact on the final frequency.

Furthermore, the maximum current available with the SOI MOS is 20% higher than for the bulk version, due to a particular undesired effect (The kink effect) described later in this chapter.

Decreased couplings

The oxide isolation has a positive impact on the noise immunity between blocks. One of the main contributors to noise is the substrate in bulk technologies. A high power, high frequency circuits such as a power amplifier may inject a fraction of their switched energy to the substrate, which may parasite sensitive parts such as amplifier inputs or analog to digital converters. The insulator provided in the SOI technology has very efficient decoupling capabilities which facilitate the embedding of incompatible functionalities within the same silicon substrate (Figure 9-9).

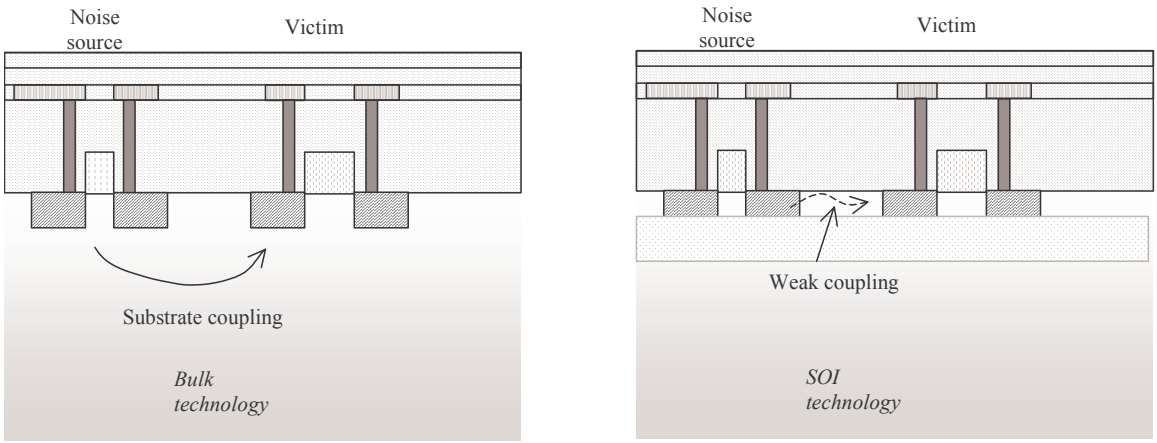
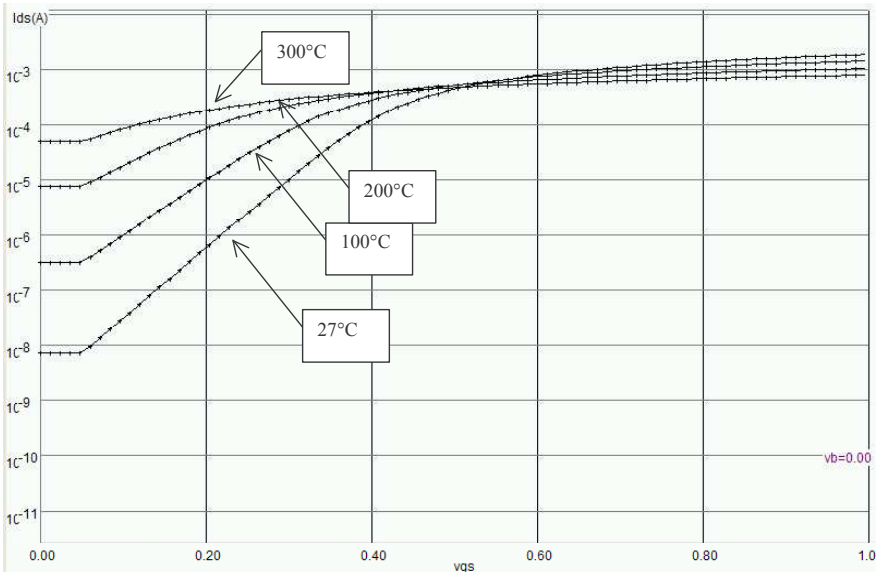


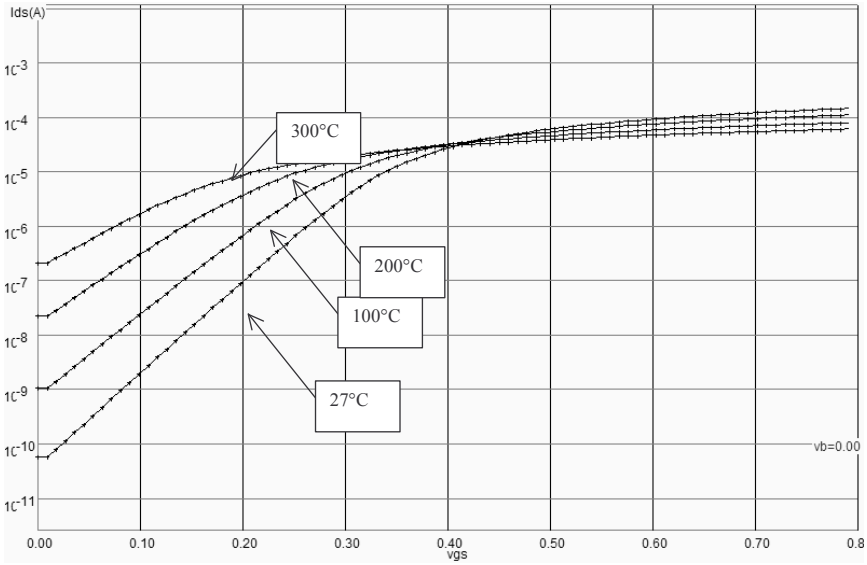
Figure 9-9: Increased decoupling between noisy and sensitive circuits thanks to the insulator

High Temperature Leakage

The *Ioff* current, corresponding to a zero gate voltage, determines the parasitic leakage current of the MOS device. A low leakage is important for low power operation. The behavior of SOI devices is better than the bulk device in terms of *Ioff* current at high temperature [1]. In the comparative simulations shown in figure 9-10, the sub-threshold slope is steeper for SOI at nominal temperature, as presented earlier. When the temperature is increased up to 200°C, the leakage current in the bulk device is rapidly increased up to 10µA, while in SOI technology, the leakage is kept below 0.1µA. Consequently, at high temperature, the SOI device has a standby current nearly 100 times lower than for bulk technology.



(a) Bulk technology



(a) SOI technology

Figure 9-10: Temperature dependence for bulk and SOI MOS devices (Low leakage W=10µm, L=0.12µm)

2. SOI technology issues

Kink effect

In SOI technology, when an n-channel MOS transistor passes strong current between the drain and the source, a parasitic phenomenon called Kink effect appears [1]. The current *Ids* suddenly rises and provokes a conductance discontinuity, usually between 0.5V and 1V in 0.12µm CMOS process. The origin of this parasitic effect is the impact ionization of high energy electrons entering the drain region, which creates supplementary positive and negative charges below the gate.

While electrons participate to the *Ids* current, the underlying insulator prevents the positive charge from being evacuated to the substrate, as it would happen in bulk technology thanks to the natural ground connection of the substrate. The positive charges accumulate below the gate (Figure 9-11). The body of the SOI MOS device may rise significantly, without any direct control. The rise of the local voltage below the gate has an instant impact on the threshold voltage which is lowered.

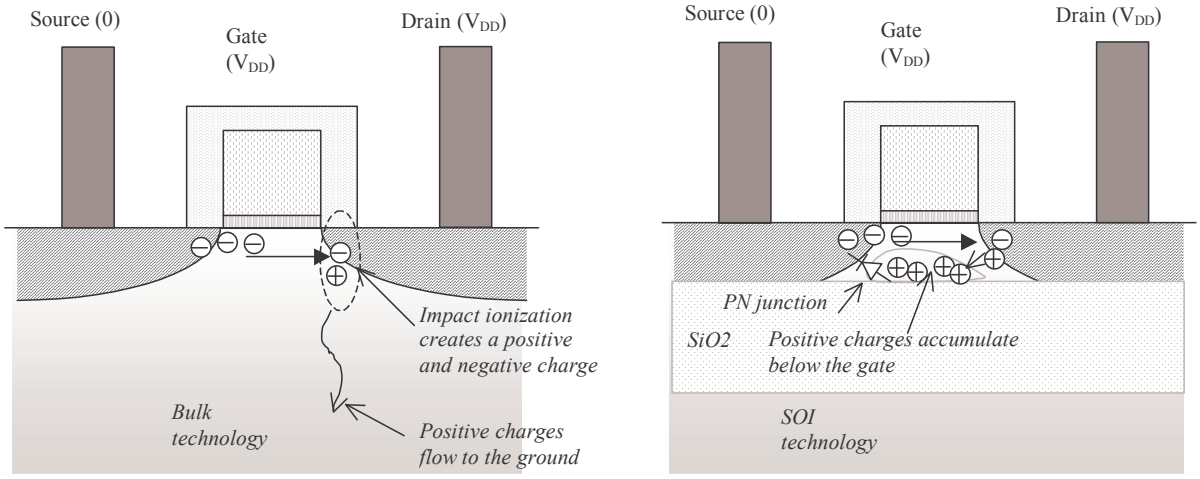
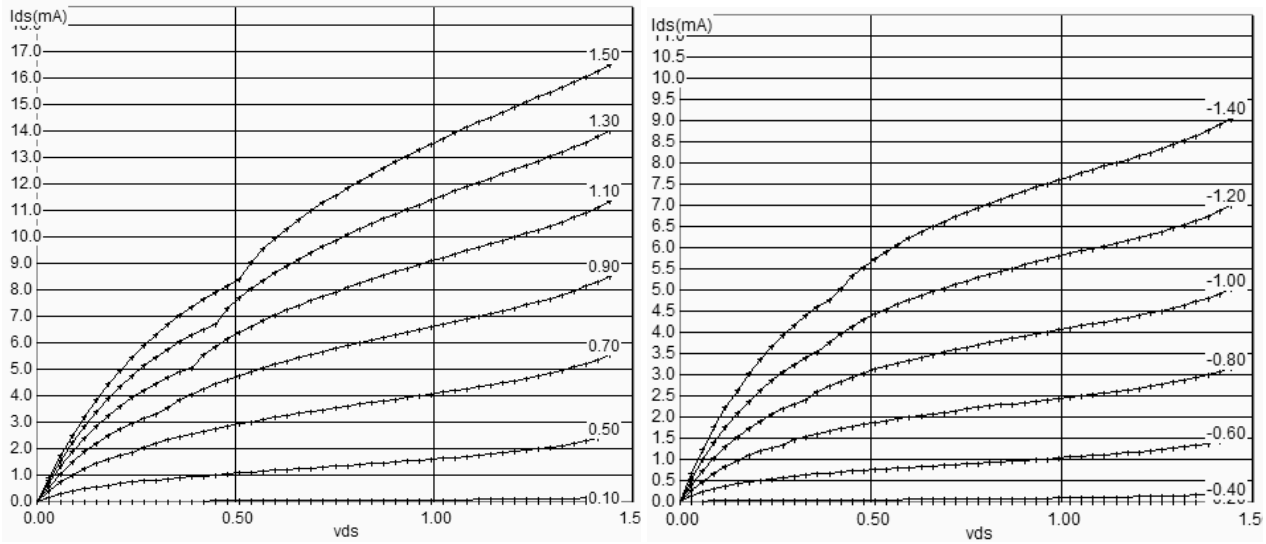


Figure 9-11: The impact ionization creates an accumulation of positive charges below the gate in the case of SOI



(a) n-channel MOS *(b) p-channel MOS*

Figure 9-12: The drain current characteristics of the n-channel and p-channel SOI devices show a kink effect near saturation

At a certain point, the bias of the PN junction between the P-doped bulk and the N+ source diffusion is high enough to turn on the junction, which leads to a sudden channel current increase, as seen in the *Id/Vd* characteristics (Figure 9-12). This effect is also called floating body effect (FBE). As the impact ionization is more severe for n-channel MOS devices than for p-channel MOS devices, the kink effect is more pronounced for the n-channel than for the p-channel.

Fully Depleted MOS

A possibility for reducing the floating bulk effect is to use a very thin diffusion for the channel, so that there is no more room for accumulation of positive charges, and consequently almost no kink effect. The source and drain diffusions are usually manufactured with an increased thickness on top of the SiO2 insulator.

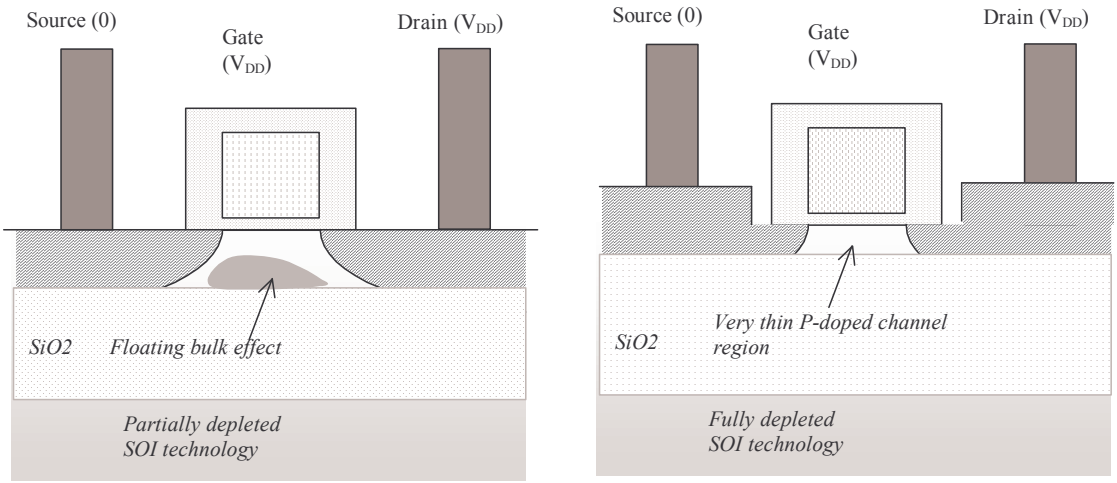


Figure 9-13: The fully depleted MOS device has no more Kink effect, but several manufacturing and design drawbacks

The fully depleted MOS devices are much harder to manufacture and control. The process-controlled threshold adjustment required for low *Vt*, high speed and ultra-high speed MOS devices is very complex due to the very thin diffusion area below the gate (figure 9-13). These drawbacks have made the fully depleted MOS less attractive than partially depleted MOS. The SOI process parameters provided in Microwind correspond to a partially depleted MOS technology.

3. SOI Device Model

Bulk silicon models such as LEVEL 3 or BSIM4 typically do not include source/bulk diode currents because the junctions are usually reverse-biased, and can be considered as junction capacitors. This is not the case for SOI devices where the source/bulk junctions can be significantly forward-biased due to the impact ionization which provokes the accumulation of positive charges below the gate.

Fully depleted MOS model

The kink effect is very weak in fully depleted SOI MOS devices. Consequently, the BSIM4 model may be applied with reasonable accuracy as the underlying physics and working principles are similar.

Partially depleted MOS model

In Microwind, the kink effect is modelized in the case of partially depleted SOI devices, thanks to a new parameter *ASOI*. Details on the SOI model in SPICE are provided in [Kuo], who considers the lateral bipolar device made of the source, the channel and the drain regions. The SOI MOS model includes a complete NPN device model in the case of an N-channel MOS, and a PNP device model in the case of a P-channel MOS. A more simple implementation proposed in Microwind consists in modifying the saturation current model directly, where the Kink effect is the most important.

The new parameter is introduced, called *ASOI*. The kink effect occurs when *Vds* is higher than the saturation voltage Vdsat. The parameter Asoi determines the amplitude of the kink. A new term is introduced, as shown in equation 9-1. This approach is a simplified version of the model used in BSIM3 SOI device model [2].

$$Ids = I_{ds\_bsim4}(1 + \frac{\mathrm{ASOI}}{L_{eff}.Vt.\sqrt{V_{DS} - V_{dsat}}}) \qquad \text{(Equ. 9-1)}$$

L = device channel length (m).
Vds= voltage difference between drain and source (V)
Vdsat= saturation voltage as defined in chapter 3 (V)
Vt = threshold voltage of the MOS device (V)
ASOI = technological parameter for handling the kink effect (default 2e6 V/cm)

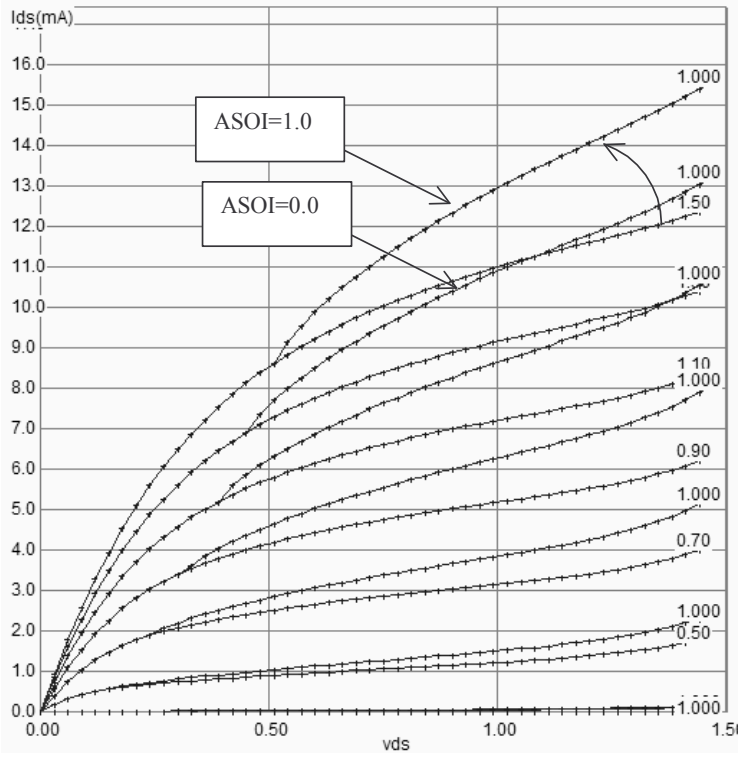


Figure 9-14: The effect of the ASOI parameter on the Id/Vd characteristics (Using soi012.RUL)

As the oxide thickness scales down to 2nm and below, the quantum mechanism of direct tunneling through the gate oxide rises exponentially. The gate current becomes large enough to compete with the channel current and consequently to affect the body potential. Much more complex models such as BSIMPD [3] have been developed for an accurate simulation of these nano-scale MOS devices (figure 9-14).

4. SOI Design

Assuming a partially depleted SOI technology, the Kink effect may be reduced by adding a polarization contact to ground which helps evacuating the accumulated charges outside the channel. The T-shape and H-shape MOS with body tie to ground are shown in figure 15. The MOS device on the left has no body contact, and may suffer from Kink effect as soon as the VDS voltage is higher than 0.5V. The T-shape MOS device includes a supplementary P+ diffusion which is connected to the P- channel region on one side and the VSS ground contact on the other side.

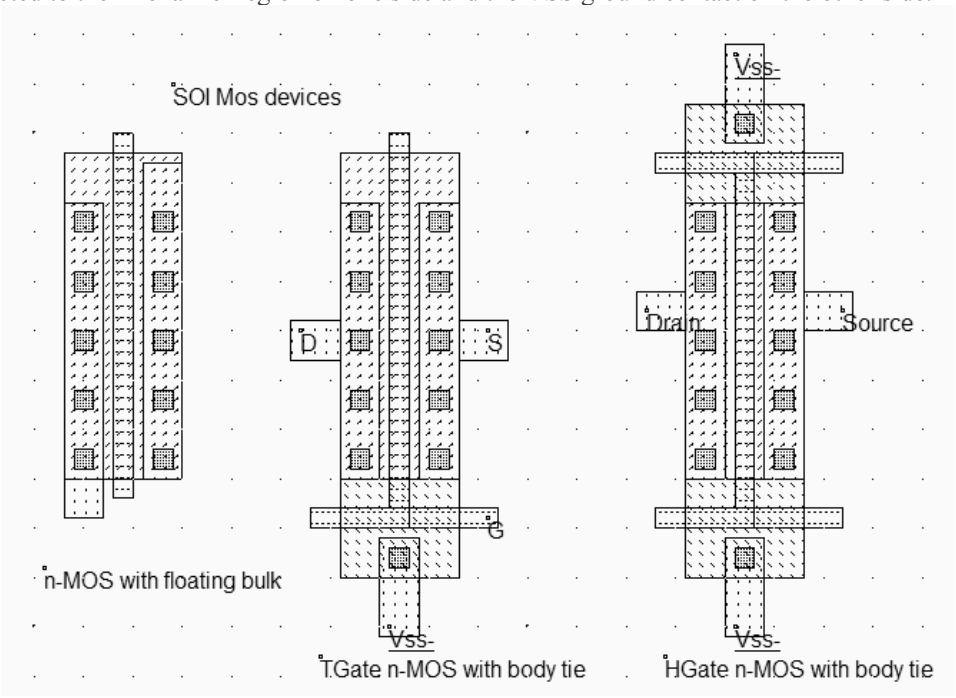


Figure 9-15: Adding a contact in partially depleted MOS to avoid the kink effect (mosSoi.MSK)

The body tie is very efficient at the bottom of the T-shape MOS but cannot evacuate charges accumulated on the upper part of the channel rapidly. An improved design (H-shape) consists in placing two body ties, one at the bottom and one on the top, which almost eliminates the Kink effect. The main disadvantage of the body tie is the important device surface increase and the needs for VSS connections at each MOS device. Important benefits of the SOI technology in terms of compact layout are lost as the body ties takes up valuable silicon space.

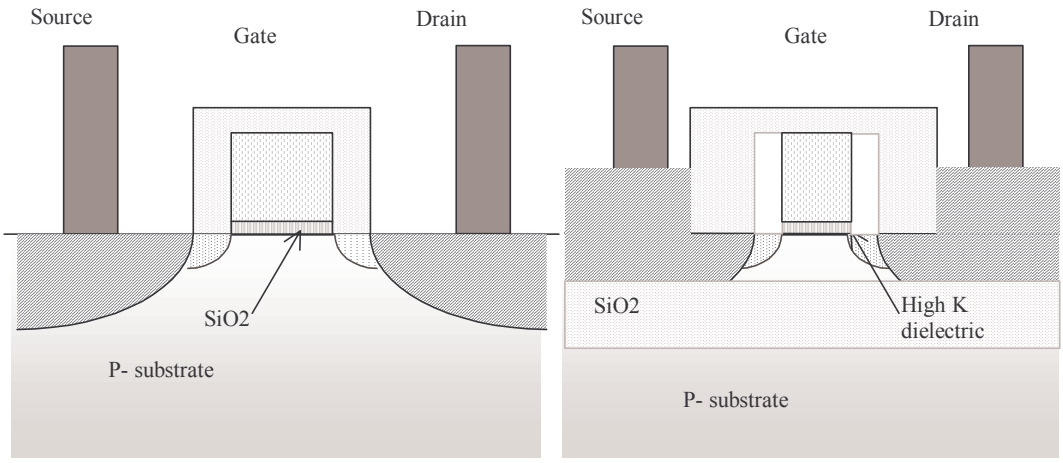
The Memory effect

Accounting for the floating body effect requires specific models which handle the "memory effect" of accumulated charges below the channel. Without body tie, the time constant for eliminating these charges is of the order of the

millisecond, far larger than the switching delay within the logic gates. However, only a very small percentage of the transistors in a typical logic circuit are unable to work properly with a floating body and require a body tie to ground. Functional error examples linked to floating body effect have been described in [1].

5. The Tera-Hertz MOS device

The Tera-Hertz (10^{12} Hertz) transistor is the key device for the development of 10-to-20-gigahertz processors. A MOS device with Tera-Hertz transit frequency is expected to be fabricated in phase with the 65nm CMOS process. The Tera-Hertz MOS device combines a SOI substrate, narrow gate length, new gate materials and a high K dielectric insulator for the gate. Technological issues to be solved concern the gate and transistor leakage currents and the reliability of the high K dielectric. A comparison between standard and Tera-hertz SOI MOS is outlined in figure 9-18.



(a) standard MOS device *(b) Terahertz MOS device*

Figure 9-18: The Tera-hertz transistor

6. Conclusion

This chapter has described briefly the SOI technology, its main advantages and drawbacks. Using Microwind, some comparison may be performed between bulk and SOI technology in terms of MOS characteristics, switching speed and power consumption. The Kink effect has been described and a simplified model has been proposed, together with body tie technique to limit its consequences. The adoption of SOI as a mainstream technology is not yet a reality, maybe because of the steady progress in bulk CMOS technology and of the drawbacks linked to Kink effect at device level. However, fully functional microprocessors utilizing SOI have recently been introduced, with impressive gains in terms of speed and power consumption, which have convinced many skeptics that SOI is a serious candidate for the fabrication of the next generation of chips.

Exercices

9-1. Design a NAND gate in SOI technology. What is the switching speed and standby current improvement as compared to bulk technology?

9-2 Redesign a basic cell (XOR, AND, Dlatch, etc..) using soi012.rul technology design rules, trying to build the most compact design. What is the surface improvement, as compared to the initial design?

References

[1] James B. Kuo, Shih Chia Lin "Low Voltage SOI CMOS VLSI Devices and Circuits", Wiley Intersciences, ISBN 0-471-41777-7, 2001

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