A proposed SRAM cell for low power consumption during write operation

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Abstract

Purpose – Low power static-random access memories (SRAM) has become a critical component in modern VLSI systems. In cells, the bit-lines are the most power consuming components because of larger power dissipation in driving long bit-line with large capacitance. The cache write consumes considerable large power due to full voltage swing on the bit-line. The aim of the paper is to propose a new SRAM cell architecture to reduce the power consumption during write 0 and write 1 operation.

Design/methodology/approach – The proposed circuit includes two tail transistors in the pull-down path of inv-A and inv-B. The simulated results of the proposed cell is compared with Conventional 6T SRAM cell and zero-asymmetric SRAM cell.

Findings – The proposed SRAM cell consumes less power than the conventional SRAM cell during write operation. The write access delay is reported to be lower than conventional and ZA SRAMs in the proposed circuit. The read operation is similar to Conventional SRAM cell but due to tail transistors the read access delay and stability is poor in the present circuit which can be improved by careful transistors sizing.

Originality/value – The paper proposes a SRAM cell to reduce the power in write "0" as well as write "1"operation by introducing two tail transistors.

Keywords Integrated circuits, Power transistors

Paper type Research paper

Introduction

The power consumption has become an important consideration on the VLSI system design and microprocessor as the demand for the portable devices and embedded systems continuously increases (Yeo and Roy, 2005; Bhardwaj *et al.*, 2001; Kim *et al.*, 2003; Senthipari *et al.*, 2006). The on-chip caches can reduce the speed gap between the processor and main memory. These on-chip caches are usually implemented using arrays of densely packed static-random access memories (SRAM) cells. Over the years, power reduction requirement in SRAM has undergone tremendous advancement (Kim *et al.*, 2005; Geens and Dehaene, 2005; Yamaoka *et al.*, 2006; Inaba *et al.*, 2006). SRAM cell includes read and write operation. Since read operation occurs more frequently than the write operation, therefore, most low-power techniques focus on reducing the power during read operation (Amrutur and Horowitz, 1994; Mai *et al.*, 1998; Morimura *et al.*, 1999; Kim *et al.*, 2004; Grossar *et al.*, 2006). The write power is usually larger than the read power due to large power dissipation in driving the cell bit lines to full swing. The power dissipated in bit-lines represents 70 per cent of the total SRAM power consumption during a write operation. Many techniques have been proposed to reduce the write power consumption by reducing the voltage swing level on the bit lines (Vkita *et al.*, 1993; Mai *et al.*, 1998; Kanda *et al.*, 2004). The boosted word-line technique (Vkita *et al.*, 1993) is a traditional solution to reduce the power consumption during the write "0" mode but it induces cell instability and hardware overheads. Half swing technique results in about 45 per cent write power reduction by reducing the bit line swing to $V_{dd}/2$ (Mai *et al.*, 1998). The main drawback of this technique is the degradation of noise margin. A proposed 7-T sense amplifying cell achieves 90 per cent power consumption reduction (Kanda *et al.*, 2004). Chang *et al.* (2004) have proposed a novel zero-aware asymmetric SRAM cell (ZA cell) to reduce the power consumption during write "0" mode only. Another proposed technique is based on hierarchical bit-line and local sense amplification (Yang and Kim, 2005) in which the voltage swing of the bit line for the write operation is reduced to $V_{dd}/10$ at the expense of additional full-swing control signals. Recently, Sharifkhani and Sachdev (2007) have proposed segmented virtual ground architecture for reducing power consumption during read and write operations. In the present paper, we have proposed a new SRAM cell to reduce the power dissipation during write "1" as well as write "0" operation. The proposed SRAM cell contains two extra tail transistors in the pull-down path of the respective inverter to avoid charging of the bit-lines. These two tail transistors are controlled by an extra signal write select (WS). During read or write mode at least one of the tail transistor must be turned OFF to disconnect the driving path of respective inverters.

The proposed SRAM cell provides lower write access delay than the conventional and ZA cell. The over all power consumption of our circuit is smaller than conventional and ZA cells. Owing to tail transistors, the stability as well as read access delay degraded in our circuit which can be improved by proper transistor sizing.

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Proposed circuit description

Figure 1 shows the circuit of the proposed SRAM cell whereas Figure 2 shows the core organization of memory using proposed SRAM cell. A block of SRAM core is composed of multiplicity of these cells arrayed horizontally and vertically and the memory core is again composed of multiple blocks.

Figure 1 Proposed SRAM cell

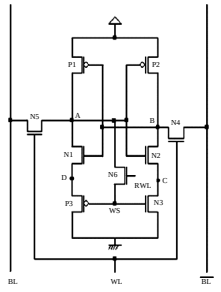
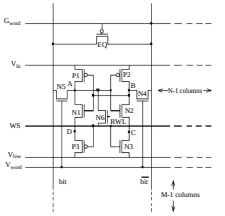


Figure 2 Memory core organization



Read mode

In the read operation, BL and $\overline{BL}$ are held at logic 1 by the precharged circuitry and RWL is always selected to high, so that signal WS is same as node voltage "A". In read 0 operation, BL starts discharging through transistors N5, N1 and P3 as shown in Figure 3(a). The sense amplifier gives output as logic 0 when BL falls below asserting voltage level (as decided by sense amplifier design). In read 1 operation, $\overline{BL}$ starts discharging through a series combination of three transistors N4, N2 and N3 as shown in Figure 3(b).

Write mode

In dynamic logic circuits, the two bit-lines are precharged initially to V_{dd}. When the write enable signal is asserted, the input data and its complement are placed on the BL and $\overline{BL}$. After that, asserting WL one can perform the write operation in the conventional SRAM cell. The bit-lines are the most power consuming components in the conventional SRAM cell because of large power dissipation in driving the long bit-lines with larger capacitance. Since, the cache write consumes considerable larger power due to the full voltage swing on the bit-lines; therefore, in the present paper we have given more emphasis on the write operation. We will consider two write operation in detail for our proposed SRAM cell. In our proposed cell, for write operation we will select RWL = 0, so that cell mainly contains 8-transistors. We will consider two write modes:

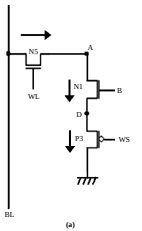
1 *Write "1" mode.* In write "1" mode, node B must be written to low that can be achieved by setting $\overline{BL}$ to "0" and asserting WL. We will consider two possible cases: Case I: writing the cell state from 1 to 1. This is not possible because both node B and $\overline{BL}$ are at zero potential. Case II: writing the cell state from "0" to one (0 → 1). In our proposed cell, it is easy to flip the cell state from 0 to 1 by setting WS = high before asserting WL.

2 *Write "0" mode.* In write "0" mode, the node B must be written to high that is done by setting BL to V_{dd} and asserting WL. Again two possible cases will be considered. Case I: write pattern is 0 → 0, since node B is initially high; therefore, this write pattern is not possible. Case II: 1 → 0. This write pattern can be easily performed in our proposed cell by setting WS = low, so that pull down path through driver transistor N2 of inv-B is disconnected. Now assert WL = high to perform the desired write pattern. This case is similar to zero asymmetric SRAM cell as proposed by Chang *et al.* (2004).

In our proposed circuit, the WS signal is used to guarantee the correct operation and by selecting proper V_{bl} and V_{low} run vertically and are generated by column drive (Ye *et al.*, 1996). Within this block, the wordline (WL) and WS of adjacent cells are connected along the horizontal axis, *BL* and $\overline{BL}$ lines are connected for all cells in a column.

Compared to the conventional SRAM cell and ZA cell, our proposed cell contains two tail transistors PMOS (P3) and NMOS (N3) which are controlled by the signal by WS. This result in a symmetrical inverter pair: Inv.A and Inv.B. These two tail transistors are used to disconnect either one of the pull-down path to flip the state of node A or B from low-to high-correctly during write operation. To avoid any reliability problem both nodes C and D should not be floating. The detailed operation of our proposed circuit is described as.

Figure 3 (a) Critical path for reading "0"; (b) critical path for reading "1"



value of signal WS before asserting WL, transition from 1 → 0 and 0 → 1 can be easily allowed. To insert WS signal before asserting WL, we have used the circuit as shown in Figure 4.

Result and discussions

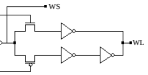
This section provides the detailed simulation analysis of the proposed SRAM cell. We first estimate the impact of the proposed SRAM cell on the power dissipation during write operation and then read and write delays.

We have simulated our proposed SRAM cell and conventional and ZA – SRAM cells by using Microwind3 and Dsch3 (Sicard, 2005) tools. All the power consumption data for three SRAM cells are obtained from the Microwind3 simulation of the extracted layout in advanced MOSIS 0.13 μm technology with a 1.2 V supply.

Access delay

- *Read delay.* Read delay is defined as the elapsed time from asserting WL to the sufficient bit line swing for correct data setting (Chang *et al.*, 2004) and the reasonable bit-line swing is 10 per cent of the full supply voltage. The read delay for read 0 and read 1 depends on (W/L) ratio of the respective tail transistors in our proposed cell.

Figure 4 The generation of WS and write wordline (WWL) signals



- *Write delay.* As discussed by Chang *et al.* (2004), the write delay is defined as the elapsed time from which the asserting WL to the states of both nodes A and B become steady. One of the tail transistors is always turned

The introduction of these two tail transistors degrades the access read delay. The read operation is similar to conventional SRAM cell but careful transistor sizing is required to maintain the same read delay as in case of conventional SRAM cell. Figure 5 shows the variation of read 0 delay varies with (W/L) ratio of tail transistor P3 for $\beta_{n3} = 3$ whereas Figure 6 shows the variation of read 1 delay with (W/L) ratio of tail transistor N3. It is observed that read 0 delay is more than read 1 delay due to presence of transistor P3 in the discharging path. In the case of read 0 mode, the delay of the proposed cell is exactly same as conventional cell for (W/L) = 4 of the tail transistor P3 whereas read 1 delay is equal for the (W/L) = 3.9 of tail transistor N3.

Figure 5 Variation of access read "0" delay with β_{N3}

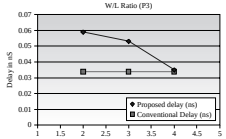


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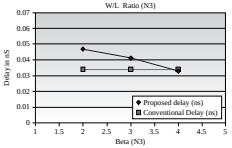
Figure 6 Variation of access read "1" delay with β_{N3}



OFF, depending upon the write mode, which disconnects the pull-down path of the respective inverters. This makes the write delay independent of the tail transistors. The write access delay for our cell and others are given in the Table I. The access delay for our proposed cell is smaller than ZA and Conventional SRAM cells.

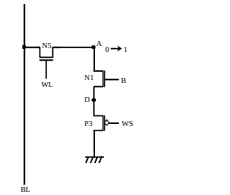
We will consider only two write patterns in detail:

1 In the case of 0 → 1, by setting WS = high and then asserting WL, the node A with initial low state would be driven to high and flip the state of node B. Figure 7 shows the path in writing cell state from low to high. Since, P3 is turned OFF in this write mode, therefore, 0 → 1, write delay of our proposed circuit is smaller than the conventional and ZA SRAM cells.

Table I Write delay (*ns*)

Write delay (ns)	Write "1"	Write "0"
Conventional	0.066	0.066
Zero-aware Asymmetric	0.059	0.052
Proposed	0.050	0.047

Figure 7 The path in writing cell state from "0" to "1"



2 In the case of 1 → 0, by setting $\overline{BL}$ to V_{dd}, WS = low and then asserting WL, node B with initial low state would be driven to high because the pull-down path of inv-B is disconnected due to N3 transistor which is OFF. This will flip the state of A from high to low. This situation is similar to the ZA SRAM cell. Figure 8 shows the path in writing cell state from 1 to 0.

The write access delay for writing 0 → 1 and 1 → 0, in all the three SRAM cells are given in Table II.

In our proposed cell, the access delay during the transition of write mode is improved approximately 46 per cent from the conventional cell for both the cases.

Write power reduction

Since, in the conventional SRAM cell, one of the two bit lines must be discharged to low regardless of written value, therefore the power dissipation in both writing "0" and "1" are the same. In contrast, the ZA cell uses the complement of input data to perform the write operation that prevents the single write bit line from being discharged if the written value is "0". Therefore, the write "0" power is far less than the write "1" power in the ZA cell. In our proposed SRAM cell, we are preventing any single bit line from being discharged during write "0" as well as write "1" mode by proper selection of signal WS which turned either P3 or N3 OFF. The simulated results of dynamic power in all the three SRAM cells, for 0 → 1 or 1 → 0 write operations, are given in Table III.

Our proposed SRAM cell dissipates lower dynamic power during the switching activity. The overall percentage reduction in power dissipation is about 90 per cent from conventional cell in 1 → 0 and 62.2 per cent in 0 → 1 whereas 62 per cent form ZA cell in 0 → 1.

Table IV shows the average dynamic power dissipation during write operations. This simulated result shows that in our proposed cell the power dissipation is lower than the conventional and ZA cells due to introduction of two tail transistors. The overall percentage reduction is 62.53 per cent from conventional and 33.31 per cent from ZA cell. The average static power dissipation during write operations in

Figure 8 The path in writing cell state from "1" to "0"

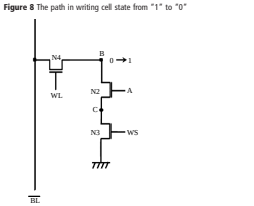


Table II Write access delay (*ns*)

	0 → 1	1 → 0	Write 1	Per cent reduction Write 0
Conventional	0.068	0.073		
Zero-aware asymmetric	0.061	0.052		
Proposed	0.047	0.050	44.68 per cent from conv. 29.78 per cent from ZA cell	46.00 per cent from conv. 4.00 per cent from ZA cell

Table III Power dissipation (μ*w*) during transitions

	0 → 1	1 → 0	Per cent improvement 0 → 1	1 → 0
Conventional	20.210	19.722		
Zero-aware asymmetric	20.191	12.570		
Proposed	12.460	10.389	62.19 per cent from conv. 62.04 per cent from ZA cell	89.84 per cent from conv. 20.99 per cent from ZA cell

Table IV Average power (dynamic and static) dissipation during write operation

	P_{avg} (μ_w)	Percentage of reduction
Dynamic power		
Conventional	17.756	
Zero-aware asymmetric	14.564	
Proposed	10.925	62.53 per cent from conv. 33.31 per cent from ZA cell
Static power		
Conventional	18	
Zero-aware asymmetric	14.4	
Proposed	10.8	66.67 per cent from conv. 33.33 per cent from ZA cell

three SRAM cells is given in Table IV. Our proposed cell again dissipates lower static power than the other reported cells. The percentage reduction is 66.67 per cent from conventional and 33.33 per cent from ZA cell.

Cell area

Table V shows the number of transistor used and area occupied on the chip in the case of three SRAM cells., i.e. conventional cell, zero-aware asymmetric cell and proposed SRAM cell.

The layout of the proposed SRAM cell is generated by Microwind3 and Dsch3 (Sicard, 2005) for 012 technology (0.12 μm) and shown in Figure 9. Our proposed SRAM cell occupies larger area on the chip but it does not compromise either power consumption or access delay. Note that the width of the proposed cell is purposely retained same as the width of the conventional and ZA cell, such that all the three cells have the same power dissipation in the word line. Most area over load is introduced by tail transistors P3 and N3 which is 27.8 per cent from conventional and 16.7 per cent from ZA cell.

Table V

	Number of transistors	Area (μm^2)
Conventional	6	13 × 11
Zero-aware asymmetric	7	15 × 11
Proposed	8	18 × 11

27.8 per cent increase from conv. 16.7 per cent increase from ZA

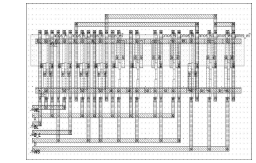
Stability

The stability is usually defined by the static noise margin (SNM) as the maximum value of DC noise voltages that can be tolerated by the SRAM cell without changing the stored bit. SNM is also defined as maximum possible square between the normal and mirrored voltage transfer characteristics (Grossar *et al.*, 2006). In the proposed SRAM cell, to compensate the stability loss due to presence of two tail transistors in pull-down path of the inv-A and inv-B, we have to enlarge (β_{N3}, β_{n2}) or (β_{p3}, β_{p3}) depending upon the mode of operation.

Conclusion

Most low-power SRAM techniques have developed to reduce only read power. Since, in the SRAM cell, the write power is generally larger than read power. The zero-aware asymmetric

Figure 9 Layout of the proposed SRAM cell



SRAM cell is designed to reduce only write "0" power. We have proposed a SRAM cell to reduce the power in write "0" as well as write "1" operation by introducing two tail transistors. Our proposed cell gives lower write access delay than conventional and ZA cells. The dynamic power dissipation in our proposed cell is reported to be lower than the other SRAM cells during write mode as well as write mode transitions. The read access delay and stability degraded due to presence of tail transistors which can be compensated by proper transistors sizing.

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