INSTITUT NATIONAL DES SCIENCES APPLIQUÉES

"Study & Modeling of Active Components" Final Report

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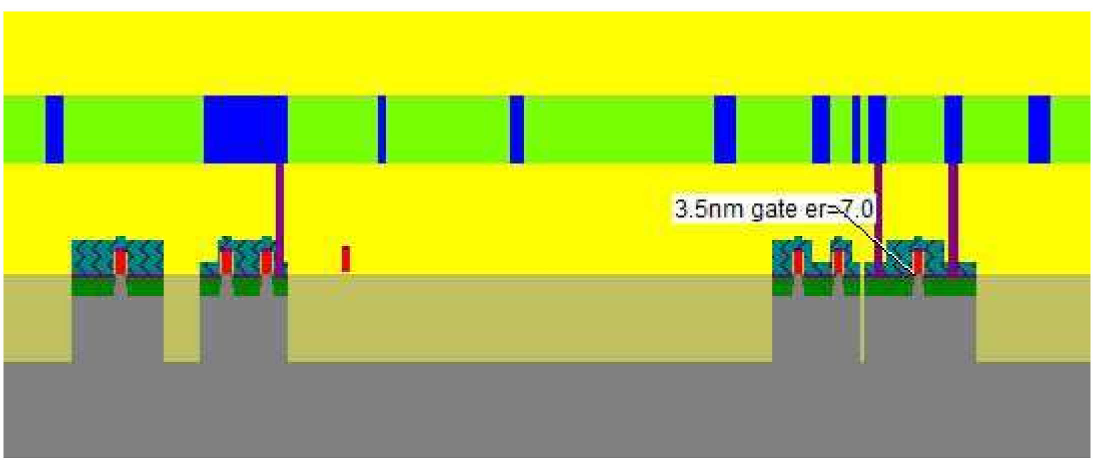


Le 26 Janvier 2015

Introduction

During the practical class, the teacher taught us the procedure to model an electronic component by using a basic boolean expression and the analysis of its behavior in different conditions (with different temperatures or input frequencies). In this repport we will present our project, including the design of the diferent parts that conform it.

Our projects :

We first made a half-adder , then a full-adder and at least a project that we called tamagochi and which involved a multiplexor 4 to 1 . There is a link between our projects, indeed we made the full-adder using the hald-adder, and our multiplexor 4 to 1 was created using several multiplexors 2 to 1. As depicted on the first part of this report, we used basical gate , implementing them on our circuits.

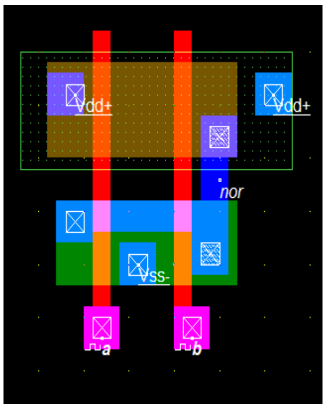
All the pictures used on our work come from the book called "Basics of CMOS Cell Design" and written by Etienne Sicard and Sonia Delmas Bendhia.

1)Basical gates

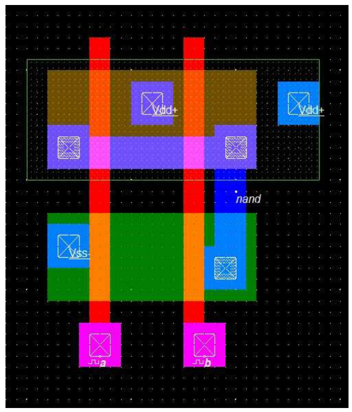
Using the CMOS logical, we use pMOS to transmit high potential and nMOS for the mass.

It is easy to make "negative" gates, therefore we start by making them, and we will use them to make their opposite with the inversor gate called NOT gate.

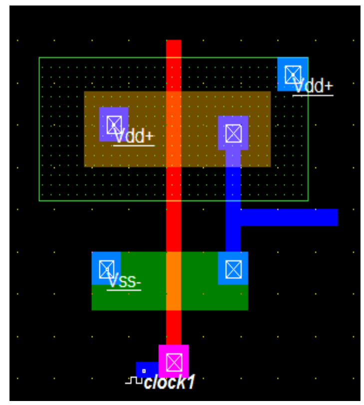
NOR gate :



NAND gate :



NOT gate :



2) Half-adder

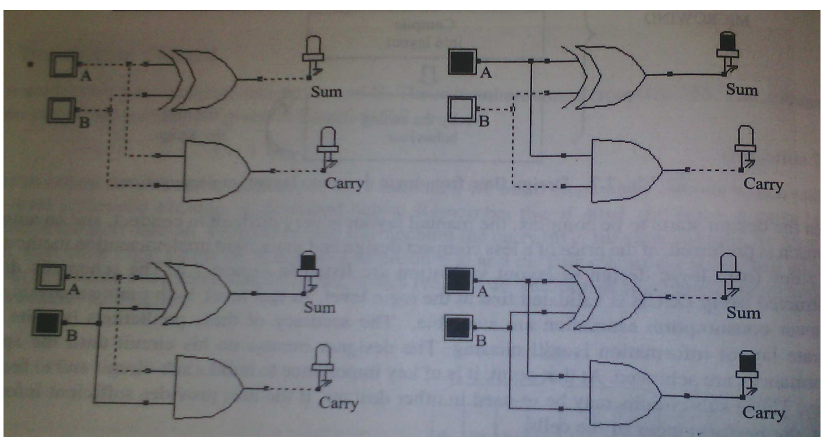
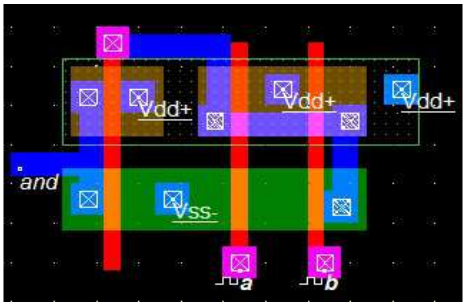


Fig. 7.8 Truth table and schematic diagram of the half-adder gate (halfAdderTest.SCH)

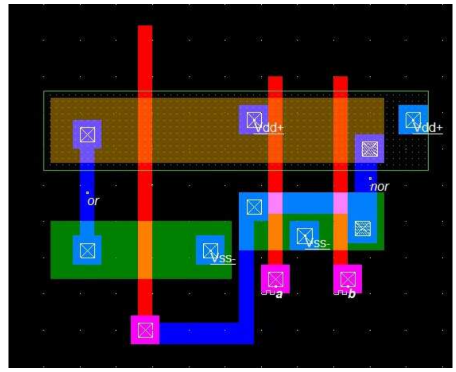
As shown on the picture, the half-adder need a AND gate and a XOR gate.

For the AND gate we connect a NAND with a NOT and we optimise the circuit to have the fastest reponse. On the same way, we made the OR gate for futur utilisations.

AND gate :

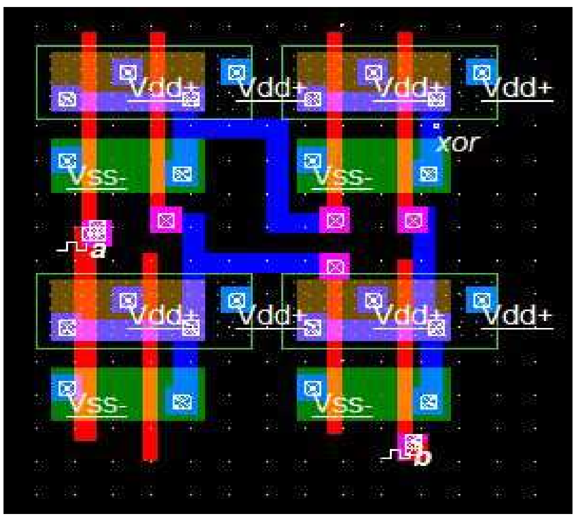


OR gate :

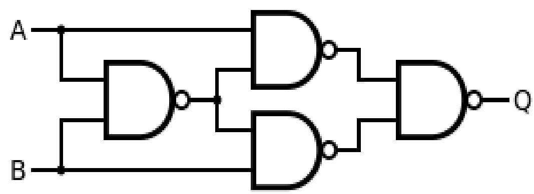


The XOR is a little more complicate, here is the scheme of the XOR gate when we create it using NAND gates and the layout we made:

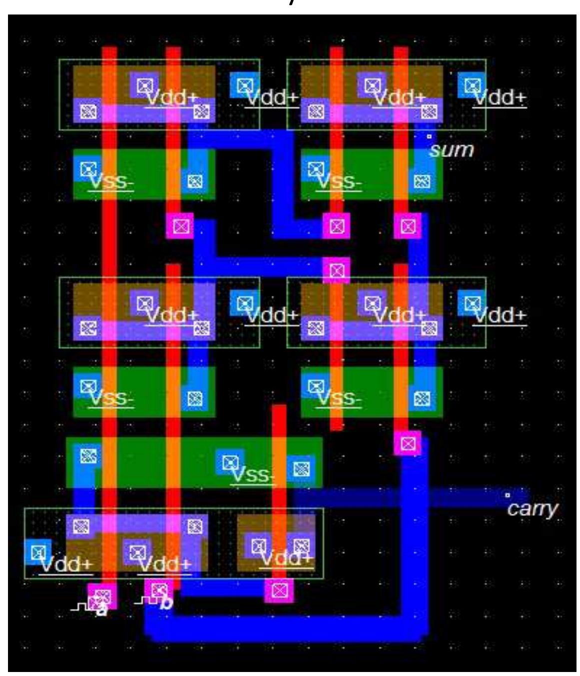
XOR gate :



XOR scheme :



Half-adder layout:



Finally, we made the half-adder

using those two gates :

the half-adder add two entries a and b

The result is seen throughout sum and

carry with the logical of the scheme

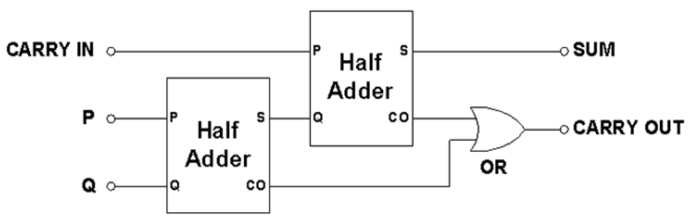
shown before.

Truth table of the half-adder :

A	B	Carry	Sum	Result
0	0	0	0	0
0	1	0	1	1
1	0	0	1	1
1	1	1	0	2

3) Full-adder

The full-adder is similar to the half-adder but permit us to add 3 entries. We have created it using two half-adders and a OR gate respecting the scheme below :

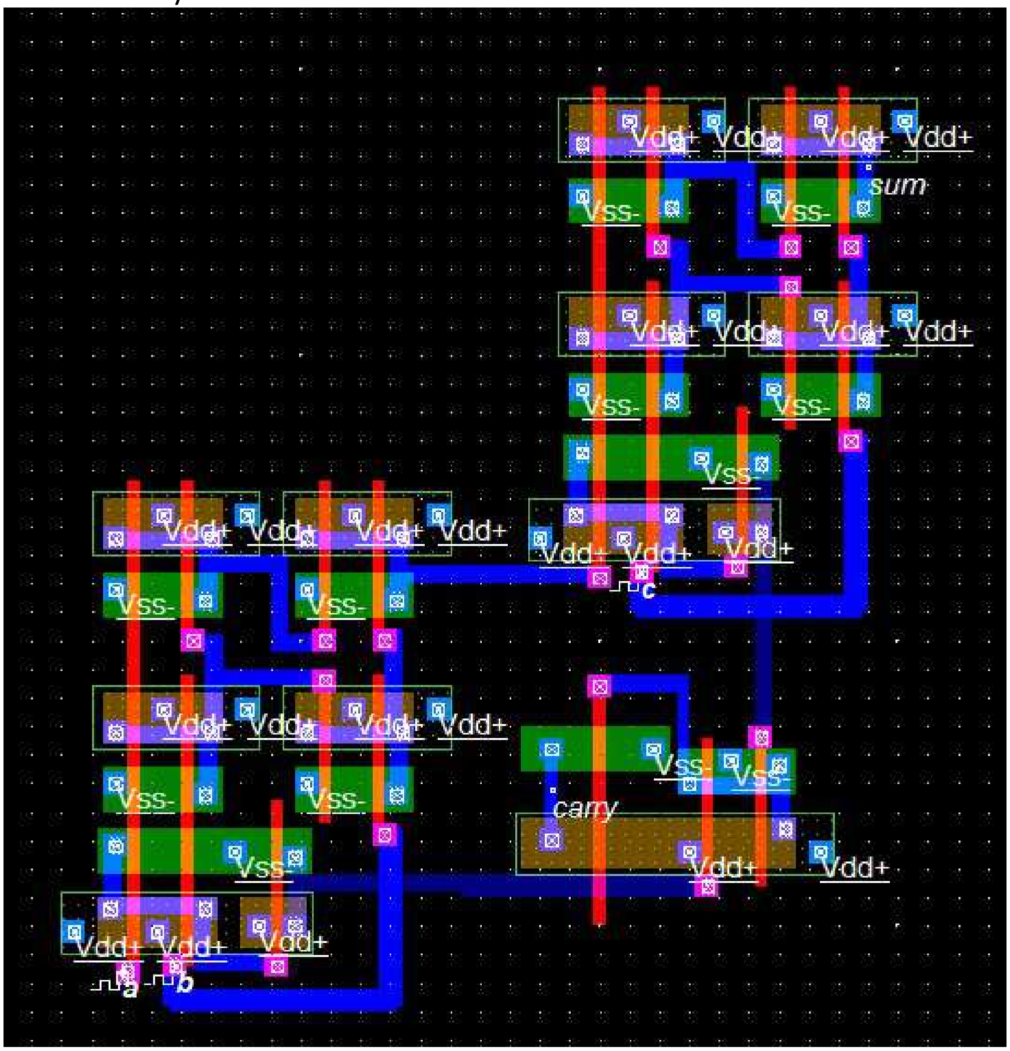


For us carry in is just a normal entry like Q and P, his purpose on the scheme is to highlight the way to do a adder with more than 3 entries. Here is the layout of our full-adder :

Truth table of the full-adder :

A	B	C	Carry	Sum	Result
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	1	1
0	1	1	1	0	2
1	0	0	0	1	1
1	0	1	1	0	2
1	1	0	1	0	2
1	1	1	1	1	3

Full-adder layout :



4) Tamagochi

For this project we had the idea to desing a circuit that react in different ways by changing the input signal like a "Tamagoshi". In our case it is a "feeding simulation game" where we have 3 different options.

4.1) How we want our tamagochi to be like

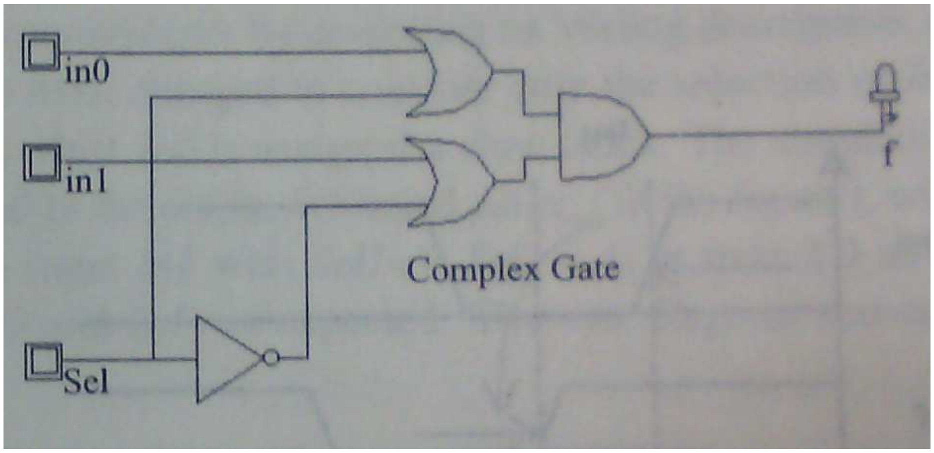
The objective is to feed a cat : an output show us the electrocardiogram's signal of the cat. If the cat is dead the signal is flat, in other hand if the cat is okay the signal has a medium frequency and if the cat is excited the signal present a high frequency.

We can feed the cat with 3 different things (3 inputs) : Honey, mouse and poison.

If we choose mouse the cat will react normally an its heart beat will be regular, if we choose honey the cat will become excited, and if we choose poison the cat will die.

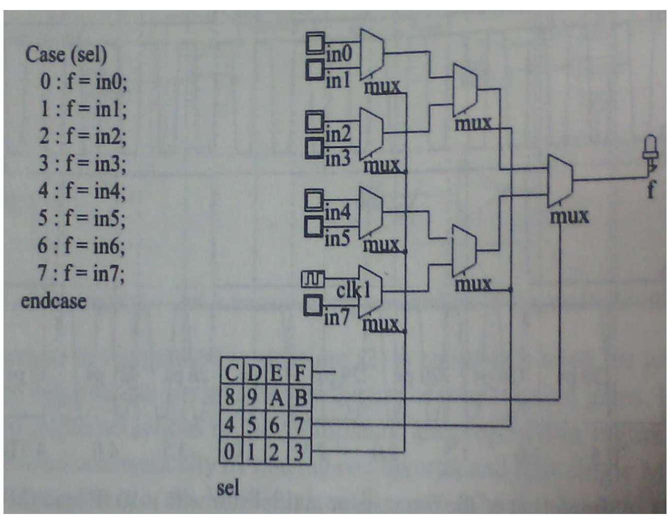
4.2) Use of the multiplexer

A multiplexer is a device that can receive different signals in different inputs and by using a system of selection we can choose the signal that we want to have in the output of the multiplexer. The next picture show one way to build a multiplexer with 2 inputs and 1 output.



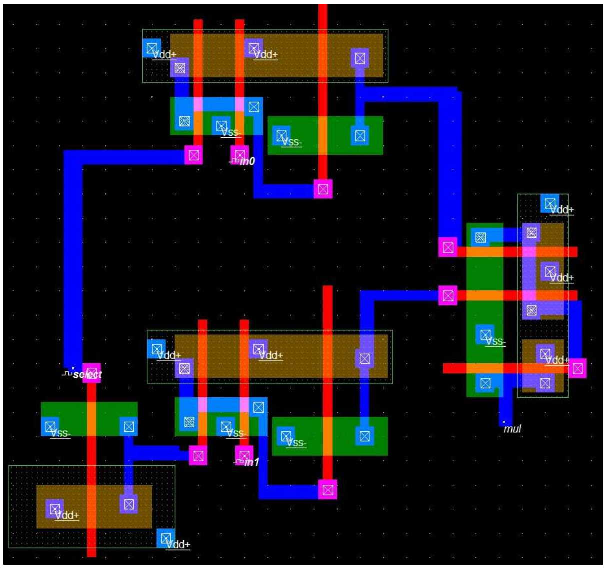
Truth table

Select	Input 0	Input 1	Output
0	X X	0 1	0 1
1	0 1	X X	0 1

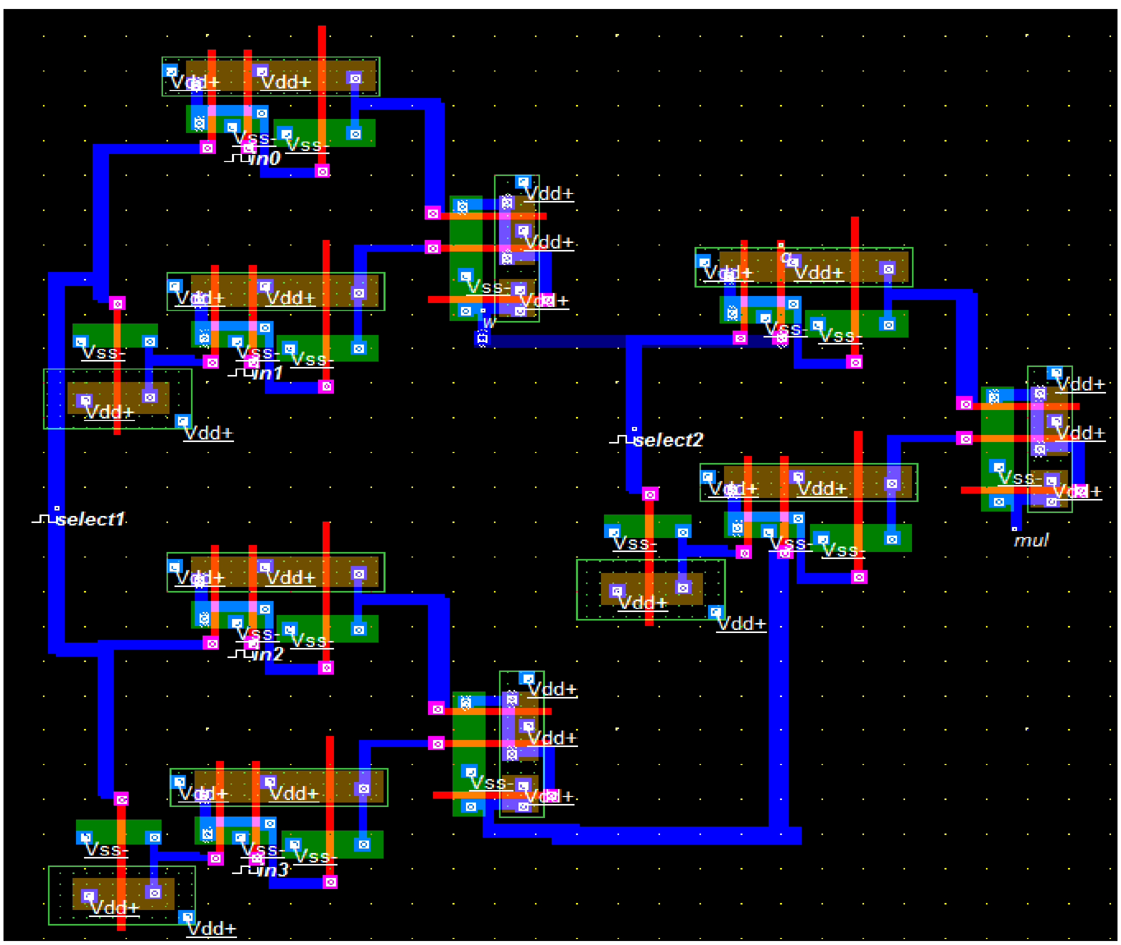


As we can see in the picture the multiplexer 2-1 is the smallest kind of multiplexer it has just one selection input but with this structure we can build more complex multiplexers, by connecting them with others (as shown in the next picture).

Layout of the multiplexer 2-1 :



Layout of the multiplexer 4-1 :



4.3)Conception of the « selection » circuits

To make this posible we made an multiplexer 4 to 1 (4 inputs, 1 output), and we used just 3 inputs: dead, regular and high for the electrocardiogram. The output is the signal selected.

The 2 select used by the 3 multiplexer 2-1 that compose the multiplexer 4-1 are described by the combinatory logic that we modelised.

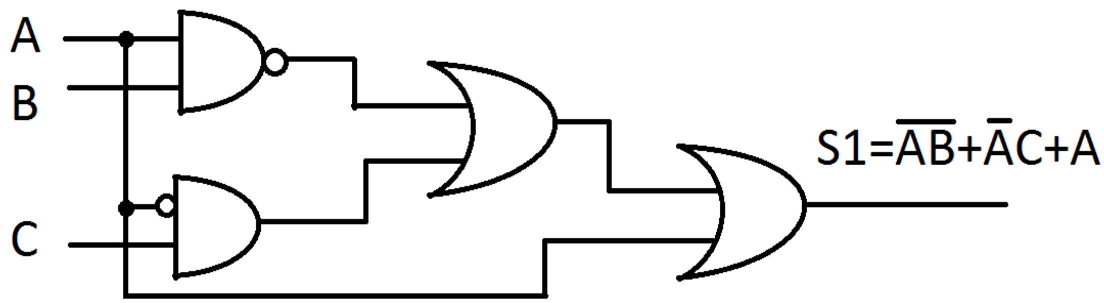
For this project we used a hierarchy system where in order of predominance for the case when the user choose more than 1 input as shown:

Poison>Honey>Mouse

Input			Signals			Select Input state	
Poison	Mouse	Honey	Slow	Fast	Dead	S2	S1
0	0	0	0	0	1	1	1
0	0	1	1	0	0	1	0
0	1	0	0	1	0	0	1
0	1	1	0	1	0	1	0
1	0	0	0	0	1	1	1
1	0	1	0	0	1	1	1
1	1	0	0	0	1	1	1
1	1	1	0	0	1	1	1

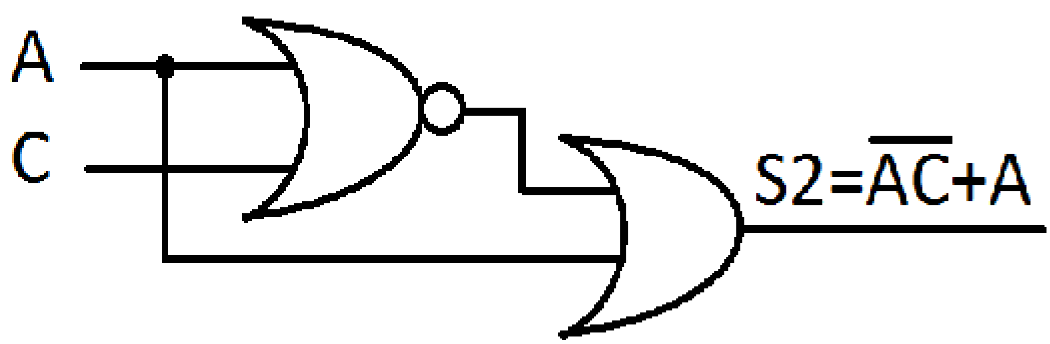
Truth table of Select 1

Poison (A)	Mouse (B)	Honey (C)	S1
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

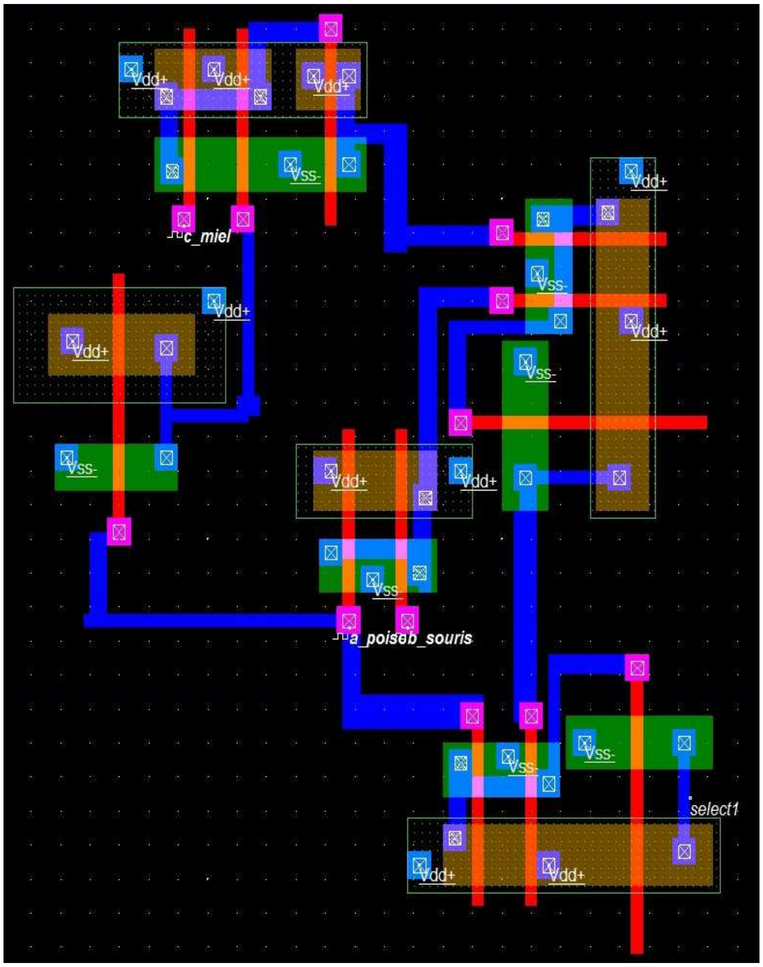


Truth table of Select 2

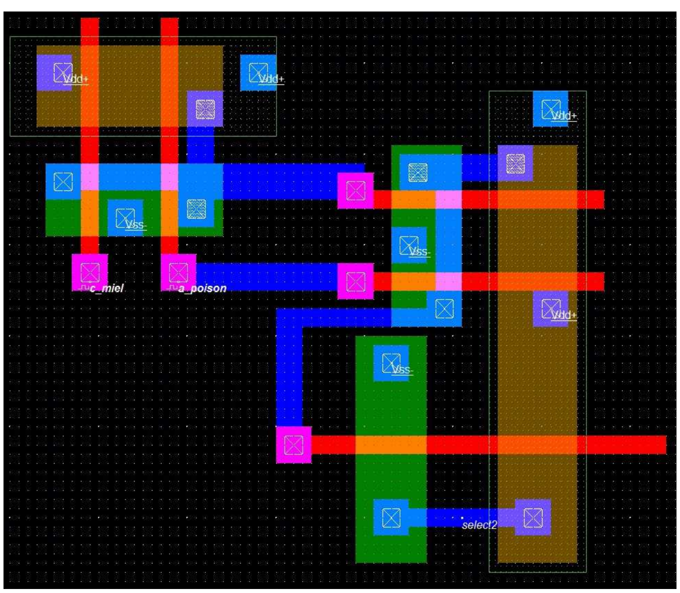
Poison (A)	Mouse (B)	Honey (C)	S2
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1



Layout of Select 1 :



Layout of Select 2 :



4.4) Difficulties encountered and how we solved them

At the beginning of our test phase, we thought that it would be easier to use continue signal as entries for the multiplexer. On the contrary, it was en error because the CMOS design only transmit 0 or +VDD at the output. Therefore we directly use clocks signals as entries, wich was the finality because it seems like electrocardiogram signals.

Moreover, we had to use higher frequencies for those entry clocks compared to those of honey, poison and mouse wich control the changes of selection. This way, iwe have been able to observ the wanted signals on the output, otherwise we would not have been able to see them due to the fast change of channel of the multiplexer.

4.5) Performance analysis

The performance of a circuit is analysed throughout his speed and the energy its consummes.

Severals paramaters influence those two caracteristics, such as the critical path for the speed.

4.5.1) Critical path

Indeed, the more a path is long, the more it will take for the signal to be transmitted, so if we want to accelerate the circuit we have to act on this path and make him softer by changing the combinatory logic of this path for example. Our critical path is between the output and the entry a_poison, and the delay is equal to 48 ps at 27 degrees. It means that we cannot use our circuit at 27 degrees with entry signals of more than 1/48 THz, that is to say 20 830 000 000 Hz. This is okay for our utilisation, because we usually do not change the entry of tamagochis this fast !

4.5.2) Influence of the temperature

Concerning the speed, the more or circuit is cool, the more its goes fast. Below is the evolution of the delay ande the consomation with the temperature.

Temperature (degrees)	Delay (ps)	Consomation (µW)
-40	36	29,5
27	48	31
125	105	38

As said before, the delay increase with the temperature.

Concerning the consomation, there is not a big influence of the temperature. Indeed, the consommation can be seen as the integral of the current, wich varations are more fast when the circuit is cooler. However the area below the current curve does not change a lot, and that is why we say that consomation is not influenced by the temperature.

Conclusion

In a nutshell, we could say concerning those projects that we learned a lot about a process wich is used in many firms nowadays. To improve our layouts we could have optimised the way the hgih potential and the mass are implemented to the circuits, using proper metals for each one. The simulations are multiple and can take in account lots of parameters such as the temperature, wich effects on the speed are important. There are many uses for the cMOS technology, in artihmetic but also in analogic components.