Input-Output Design in a 45nm Small Microprocessor Using Microwind

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***Abstract*— This paper presents the development of input-output (I/O) structures in a very small 45nm technology microprocessor. A process, voltage, temperature (PVT) testing is done with the device performance validation. The analysis and every module validation is developed in Microwind.**

I. INTRODUCTION

The central process of any device is done on the microprocessor [1]. The characteristics of a microprocessor depends on the application field, where in general there is a trade-off between power consumption, size and speed, just to name a few. Certain devices must support extreme conditions so it is necessary to test the microprocessor and its modules in this conditions to ensure a right performance. The total microprocessor size mainly depends on the technology, module size optimization and the number of bits that will be used. Moreover, one of the most important tasks is to establish the communication with other devices. The input-output interfacing enables this task. The inputs are composed of protection pads for the electrostatic problem and high voltage, while the output is focused on the signal amplification so the signal can be read and manipulated at the outside [2].

This paper briefly describes in the section two and three the fundamental modules such as 4-bit Adder (ADD4bit) and Counter. The first one is one of the basic operations used in an Arithmetic Logic Unit (ALU). And the counter module is used in the clock module which feeds the microprocessor and all the operation on it. On the other hand, in section four is presented the Input-Output and internal structures designed to interact with external environments. In each section is explained the function, schematic and layout implemented, where the layout will be built by the designer criteria. The final section presents the performance of the designed modules. This is a 1 week project part of the Master Nanoelectronics program. The purpose is to establish the communication between the chip and the external world. For that, we are based on simulations using Microwind.

II. 4-BIT ADDER

This module is a simple block which performs the sum operation by using 4 Full Adders connected in series where the carry propagates through them. For simplicity, the design is done for 4 bits. The layout design considers the minimal dimensions for most of transistors but the transistor width were increased where the carry propagates. This is done in order to obtain a good response in the raising and falling time of the output signal.

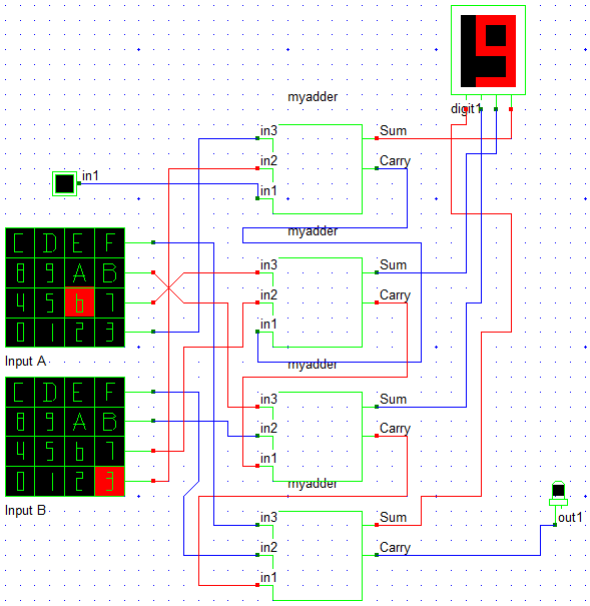

Fig. 1. ADD4 Schematic Configuration

III. COUNTER

The counter is asynchronous and is designed to accomplish the function of a frequency divider. The clock is a synchronous signal used with this frequency divider in order to operate at a certain frequency, where this operation frequency is chosen depending on the application. This is a 4-bit counter where a reset signal is controlled according the desired design. In the next subsections it is presented the schematic and layout.

The counter schematic is composed by D-Registers (D-reg) which are based on inverters. The D-reg are placed in series where the number of bits depends directly on the number of D-reg. On the other hand, the counter layout design is done by using the minimal dimensions according to the technology. Furthermore, the source and ground connections were established in the metal-2 layer.

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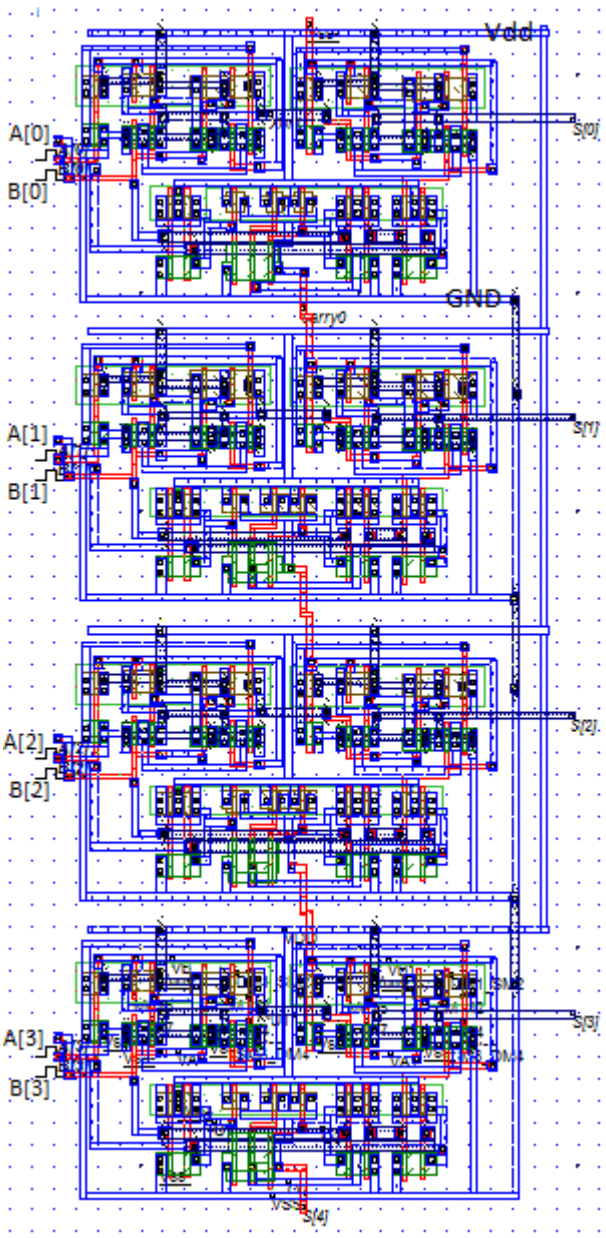

Fig. 2. ADD4 Layout Design - Column Orientation

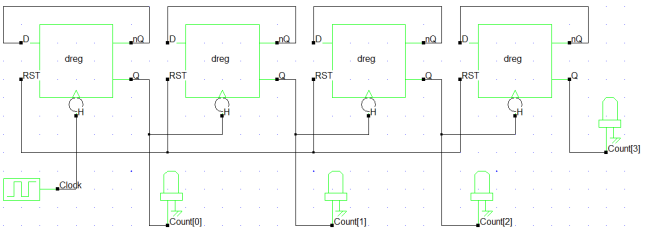

Fig. 3. Counter Schematic

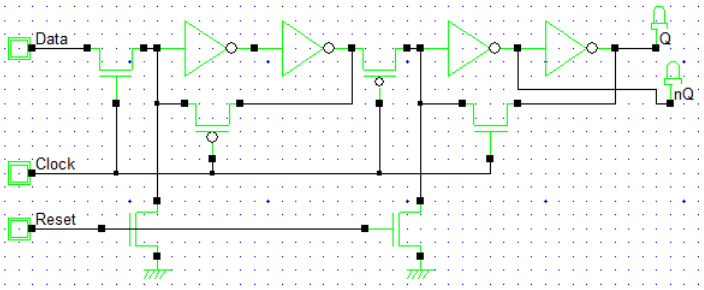

Fig. 4. Dreg configuration using inverters

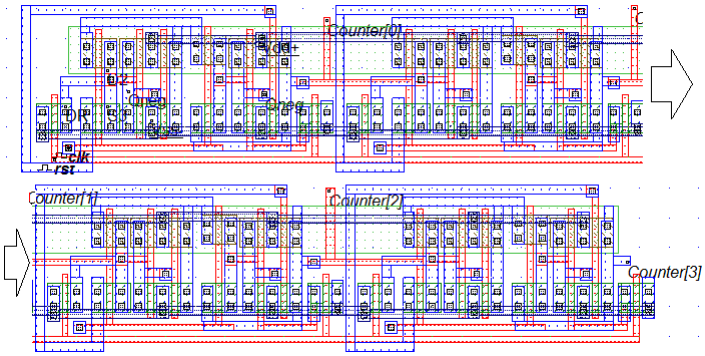

Fig. 5. Counter Layout Design - Row Orientation

IV. INPUT-OUTPUT (I/O) MODULES

To communicate with external environments, bonding Pads, buffers, converters and protections must be designed. The output data passes through structures that are designed for high voltages while the input data through internal ones for low voltages. So, a voltage conversion between low and high voltages is necessary. We have two types of supply voltages: High voltage ($V_{dd-high} = 1.8V$) and low voltage ($V_{dd-low} = 1V$). This values satisfies the 45nm technology. Figure 6 contains the general paths that allows the communication.

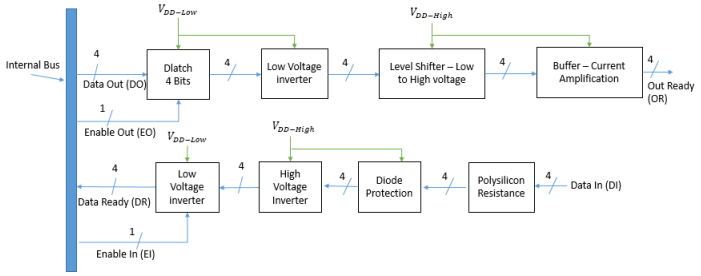

Fig. 6. General Input-Output Paths

A. I/O Structures

Input structures are conformed by a conversion from low to high voltage or vice versa and should be protected from high voltages, so it is only permitted a 1 V input. 7 and 9 shows the schematic and its layout. The input path is conformed by three sub-stages: a PolyResistor, a protection

diode and a high to low voltage conversion. First and second stage help to protect from high voltage input (greater than 1.8) and the last stage supports the $V_{dd-high}$ and delivers the appropriate V_{dd-low}. For this, it is necessary the use of robust diodes and transistors.

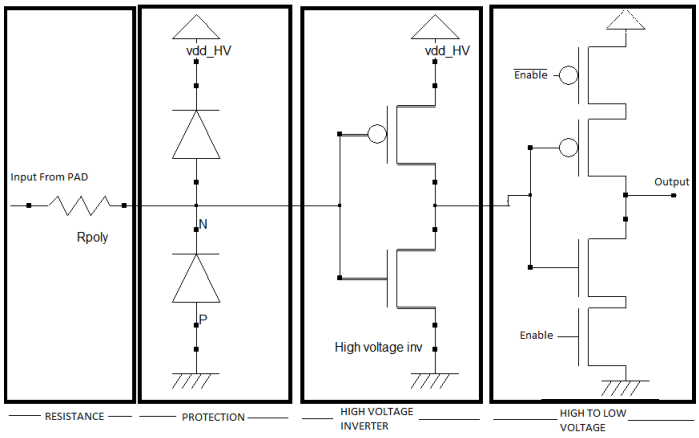

Fig. 7. Input path schematic

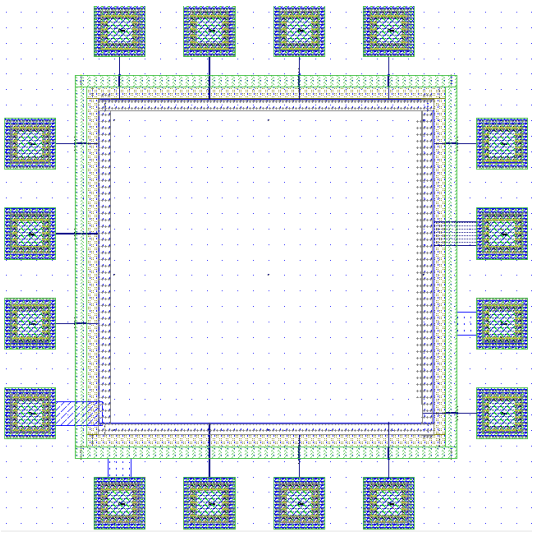

Fig. 8. Chip General Structure. For practical purposes it is presented the chip without the connection to other modules. Three ring pads are present: one for V_{SS}, V_{DD} and $V_{DD-High}$

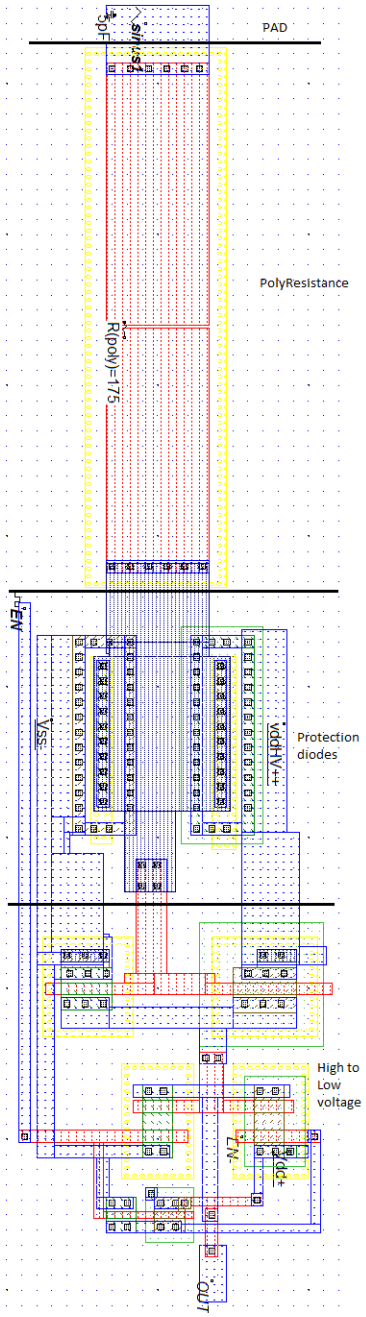

Fig. 9. Input Pad Layout. Three stages are present and a 5 pF capacitor simulates an input pad interaction

On the other hand, the output path structure has three sub-stages: the latch stage, a level shifter stage and the buffer stage. The first stage stores the information and delivers it to the output when an enable signal is sent. The amplification put the output to 1.8 V (level shifter) and the buffer amplifies the data. Figures 10 and 11 shows these structures.

B. Protections and PADs

PADs are used for input and output connection signals where the size of each PAD is $50x50\ um$. Furthermore, protections should be presented in each PAD except for the radio frequency (RF) output PAD because the signal should be present with full power in order to transmit data. In figure

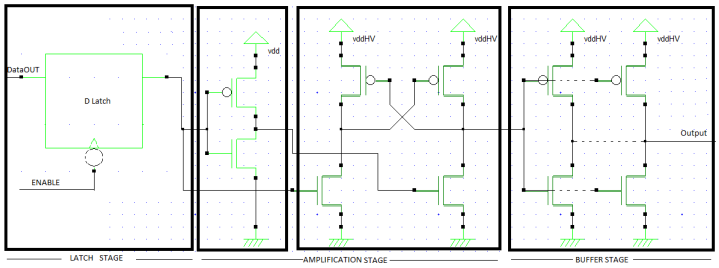

Fig. 10. Output path schematic

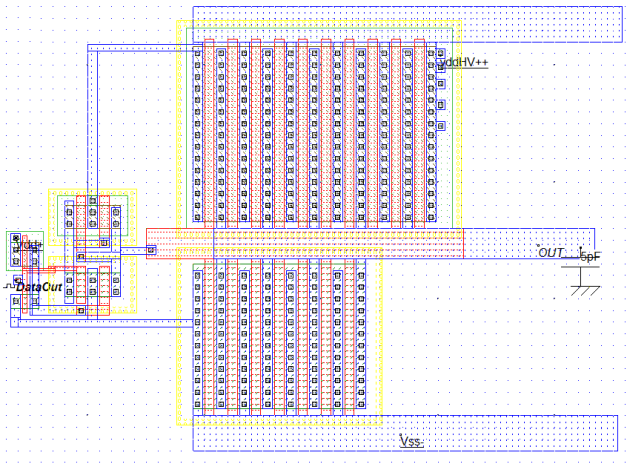

Fig. 11. Input data schematic. For simplicity the latch module were omitted

8 we can see the chip with 16 PADs and in figure 12 is shown the protection diodes.

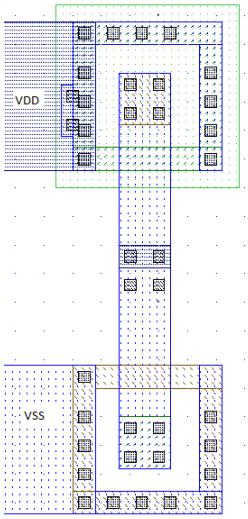

Fig. 12. Chip General Structure. For practical purposes it is presented the chip without the connection to other modules. Three ring pads are present: one for V_{SS}, V_{DD} and $V_{DD-High}$

V. Performance and Validation

In the table 1 is presented the characteristics of the implemented modules. The results were extracted from simulation where the modules were under PVT conditions. Furthermore, in figure 13 is presented the validation for the 4 bit input path (critical path).

VI. Conclusions

The microprocessor is composed by various modules that accomplish important functions to control precisely the information. One of the fundamental modules is the clock which is the heart of the microprocessor. It controls all the actions and make a synchronous operation enabling the user to manipulate correctly the data. Then we have the ALU where

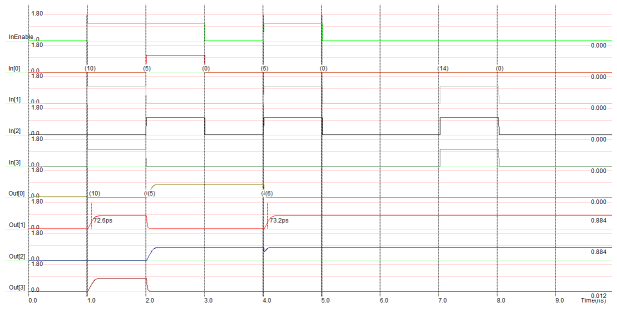

Fig. 13. Input PAD simulation. The external inputs are 10, 5 and 6 for A, B and RF input respectively and as chip inputs we have the same values. This response validates the input path.

TABLE I

Performance of the Designed Modules

	PVT Conditions		
Temperature $[°C]$	-50	27	125
Counter	Maximum	Typical	Minimum
Maximum frequency $[GHz]$	17.2	12.5	7.7
Power $[\mu W]$	196	88.9	34.5
ADD4	Maximum	Typical	Minimum
Maximum delay $[ps]$	222	238	267
Power $[\mu W]$	54.3	36.4	40.8
Output Path	Maximum	Typical	Minimum
Maximum delay $[ns]$	0.89	1.5	3
Power $[mW]$	2.1	1.8	1.5
Input Path	Maximum	Typical	Minimum
Maximum delay $[ps]$	35	36	49
Power $[\mu W]$	41	14.1	5.4

all the basic operations are present. Finally, I/O structures and PADs present important modules to help the communication on external tasks and devices. For this goal is important to deliver and receive the pertinent information, also a right protection is needed in each PAD. The performance is appropriate to general microprocessor conditions. Despite the fact that the microprocessor manipulates a low number of bits, it can be upgraded and optimized in each module. Each module where validated by simulation but the final designs does not follow perfectly the design rules. Also the modules has not been connected between them in the final chip. In the next step, it is necessary to accomplish this missing tasks and simulated it in order to validate the final design. On the other hand, this can be done with other technology so the chip space can be optimized.

References

[1] M. R. Betker, "The History of the Microprocessor," Bell Labs Technical Journal, Autumm, 1997.
[2] Sicard. E, "Input Output Interfacing," in *Advanced CMOS Cell Design*, USA: McGrall-Hill, 2007.