Program Counter and Instructions Decoder for a chip design

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***Abstract*—This paper will present the main characteristics of 4 circuit layouts designed and simulated with Microwind and with a technology of 45 nm (8 bit program counter, instructions decoder, 4 bit adder and 16 bit counter) as part of the basis for a chip design. It also contains the analysis of results in three different cases: typical case, worst-case scenario (high temperature, low voltage) and best-case scenario (low temperature, high voltage).**

***Index Terms*—**Decoder, D register, Counter, Layout.

I. Introduction

The program counter and the instructions decoder are circuits that work closely with the memory. While the decoder reads the instructions from the memory and give the enabling pulse to the other circuits, for example the ALU, inputs and outputs and RF circuit, the counter will work as a primitive clock for the entire chip. However, in first instance, there was necessary to do an analysis of the simulation for the 4 bit adder and 16 bit counter, to have a preview of the layout designing process and the results of their simulations.

II. 4 bit adder and 16 bit counter

For the construction of the 4 bit adder, it was necessary to understand first the functioning of the Full Adder. Two XOR connected to the three inputs perform the sum while 4 NANDs perform the carry of the adder.

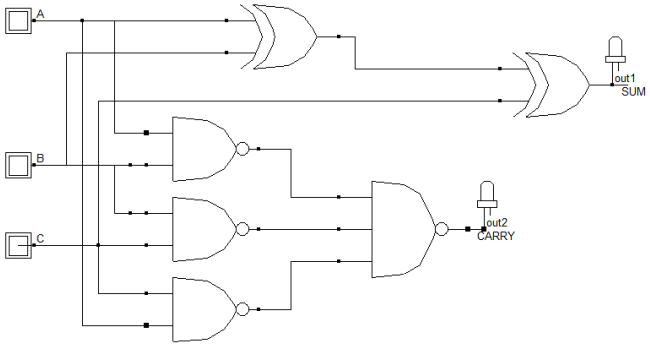


Figure 1: Schematic of a Full Adder

A. 4 Bit Adder

This circuit consist in 4 full adders. Each first input, represents one bit of the input B and each second input of each full adder, is connected to one bit of the input A. Every carry output is connected to the last input of the previous full adder module. The simulation of the schematic was performed with DSCH software in order to understand or to verify the functioning of the circuit.

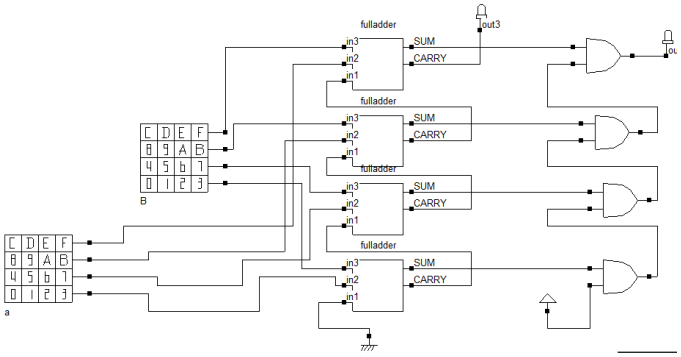


Figure 2: Schematic of the 4 bit adder

The simulation of the Layout shows a delay of 0.31 ns in a typical case scenario (25ºC and Vdd of 1 V).
This design showed a minimum voltage of 0.4V in Vdd. For voltages less than that, the circuit did not work properly.

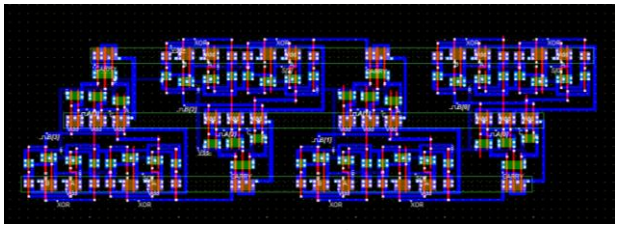


Figure 3: Layout of the 4bit adder

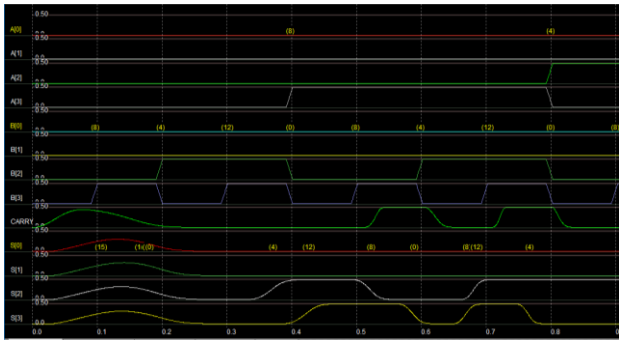


Figure 4: Simulation of the 4bit adder

When evaluating the frequencies for all the cases, the frequency didn't present a major difference among them. The worst-case scenario values are inside the tolerance margin of functioning.

TABLE I
SIMULATION VALUES FOR THE FOUR BIT ADDER

	Typical	Worst case scenario	Best case scenario
Delay [ns]	0.31	0.32	0.306
Frequency[Ghz]	4.82	5.01	4.9

B. 16 Bit Counter

The design of the counter includes 4 D registers in series. Comparing to the adder, the counter has a greater initial delay. The frequency of this design is around 0.4 GHz and the minimum voltage in Vdd is about 0.6 V. The simulation for the three different cases are shown in table 2.

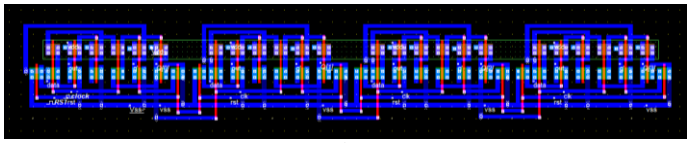


Figure 5: Layout of the 16 bit counter

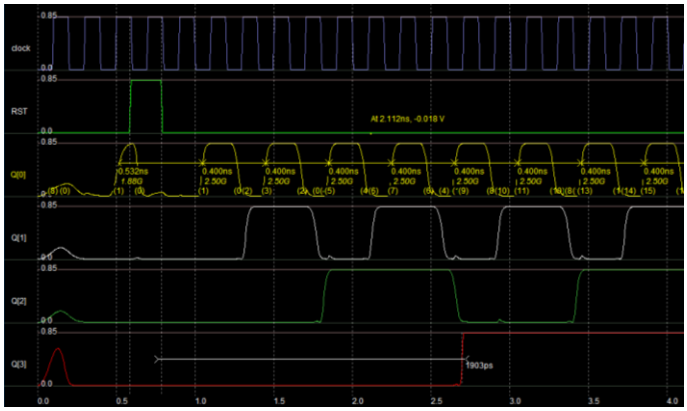


Figure 6: Simulation of the 16 bit counter

TABLE II
SIMULATION VALUES FOR THE 16 BIT COUNTER

	Typical	Worst case scenario	Best case scenario
Delay [ns]	1.78	1.9	1.55
Frequency [ghz]	0.4	0.39	0.44

III. 8 BIT COUNTER AND DECODER

The 8 bit counter performs the clock of the entire chip. The memory will give the instruction to the decoder on every positive edge of the counter. After receiving the instruction, the decoder will send pulse signals to enable every other circuit inside the chip.

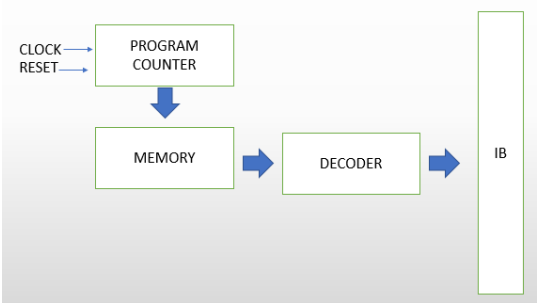


Figure 7: Flow Diagram of the Program Counter and Decoder inside the chip

A. Program counter

The design of the program counter has a similar structure with the 16 bit counter but only three D registers where took in consideration, as shown in figure 8.

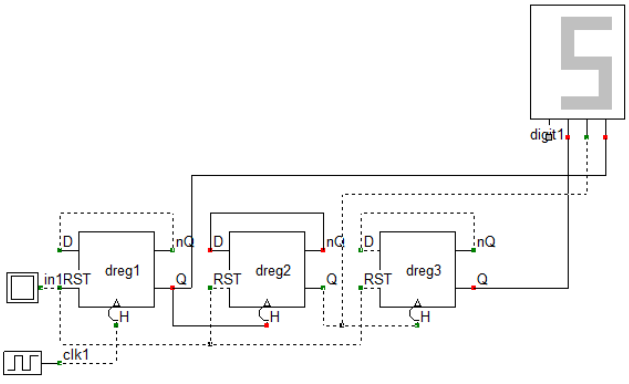


Figure 8: Schematic of the 8 bit program counter

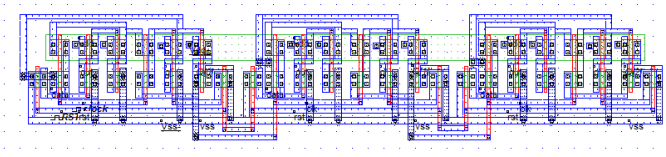


Figure 9: Layout of the 8 bit program counter

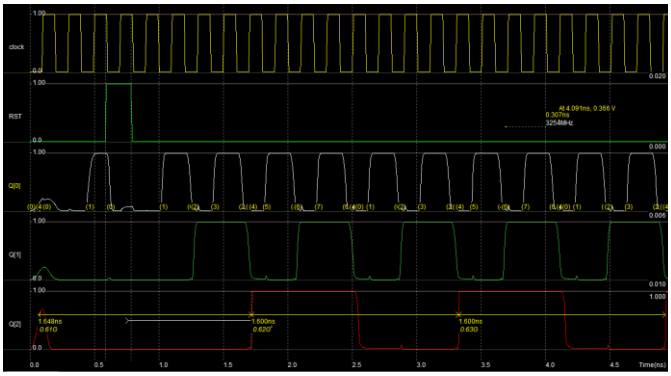


Figure 10: Simulation of the 8 bit program counter

The simulation results shows that the design will give a clock of 0.4 ns for the functioning of the entire chip and an initial delay time of 1.68 ns. The table 3 gives other important values from the simulation.

TABLE III
SIMULATION VALUES FOR THE 8 BIT PROGRAM COUNTER

	TYPICAL	Worst case scenario	Best case scenario
Start Time [ns]	1.648	1.705	1.429
Delay [ns]	1.6	1.6	1.6
Frequency [ghz]	0.63	0.63	0.63
Power [uW]	57.091	27.248	143
Voltage [V]	1	0.85	1.15

B. *Instruction Decoder*

The decoder was built according to the table of instructions shown in figure 11.

TABLE OF INSTRUCTIONS

C2	C1	C0		ENABLE ALU	ADD	SUB	COMP	STORE A	STORE B	OUT ENABLE	IN ENABLE	RF ENABLE	ENABLE A	ENABLE B
0	1	1	IN A	0	0	0	0	1	0	0	1	0	1	0
1	0	0	IN B	0	0	0	0	0	1	0	1	0	0	1
0	0	0	ADD	1	1	0	0	0	0	0	0	0	0	0
1	0	1	IN TO RF	0	0	0	0	0	0	0	1	1	0	0
0	0	1	SUB	1	0	1	0	0	0	0	0	0	0	0
1	1	0	OUT R	1	0	0	0	0	0	1	0	0	0	0
0	1	0	COMP	1	0	0	1	0	0	0	0	0	0	0
1	1	1	R OUT RF	1	0	0	0	0	1	0	1	0	0	0

Figure 11: Table of instructions

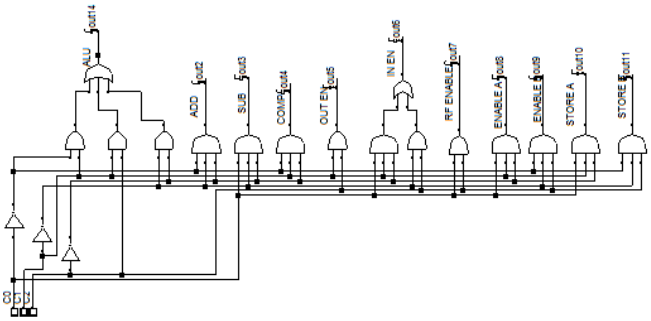


Figure 12: Schematic of the Instructions Decoder

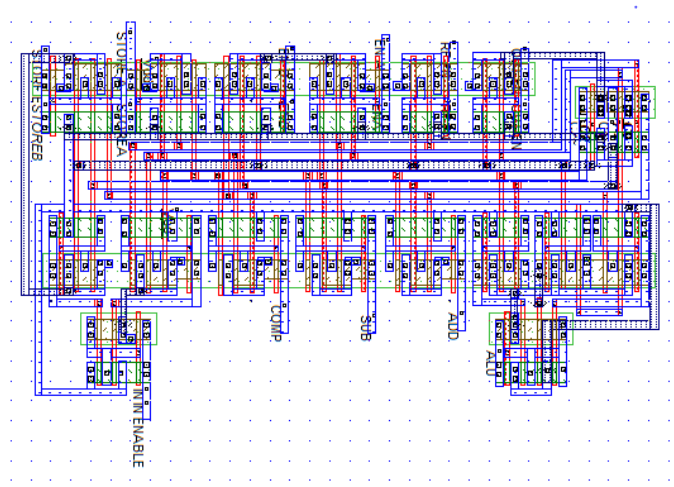
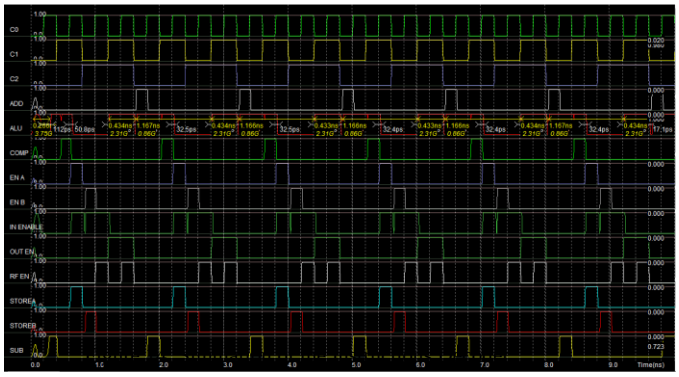


Figure 13: Layout of the Instructions Decoder

The decoder sent a pulse to enable three different circuits in the chip: the ALU, input and outputs and RF circuit.

For this project, the decoder had just eight different instructions from the SRAM, the decoder and the rest of the circuits were connected to an internal bus (IB). At the same time, the internal bus was configured with some specific values for the input and output in order to test each one of the circuits.



IV. Conclusion

In order to have a working chip, it is mandatory to discuss the main specifications of each circuit and to avoid inconsistencies among circuits.

The performance of the layout of a circuit depends on the design itself. The compliance of the lambda rules was mandatory to obtain better result on delay, frequency and power dissipation.

References

[1] E. Sicard, S. Delmas-Bendhia, “Arithmetics”, in *CMOS Circuit Design, Simulator in hands.* Ed. Mc Graw Hill, India.